# Smart SR Converter HYC9012

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# Smart SR Converter HYC9012

## Features

- SR Controller
  - Low-side synchronous rectification without auxiliary winding
  - Supports Multi-Mode operation: DCM, CCM, PFM and QR
  - Wide output voltage range:3.0V-25V
  - VDD bias clamped at 8V
  - 4.8V Minimum VDD for VIN>3.0V
  - Adaptive pre-turn off driver speeding up turn off transition
  - Shoot through protection(STP)
  - Optimized switching loss and EMI
  - Low quiescent current
- SR MOSFET
  - 9mΩ $R_{DS\_ON}$
  - 100% avalanche tested
  - 100V $V_{DS}$ break down
  - Pb-free lead plating, RoHS compliant
  - Halogen-free according to IEC61249-2-21

## Description

HYC9012 is a high integration smart digital control synchronous rectifier controller together with SR MOSFET in one package. It drives the standard N-channel power MOSFET to replace Schottky in order to achieve the high efficiency. HYC9012 incorporates the digital control technology to optimize the multi-mode operation at DCM/PFM/CCM/QR in the different applications. The digital control technology further enhances the robust CCM operation. Adaptive pre-turning off scheme not only guarantees the fast transition but also minimizes switching loss. The adaptive pre-turnoff scheme optimizes the EMI due to the soft SR MOSFET switching off transition. HYC9012 integrates 9mΩ SR MOSFET to minimize the external BOM and optimize the system performance.

HYC9012 is available with SOP8 package.

## Applications

- USB PD and Quick Chargers
- AC/DC offline adaptor



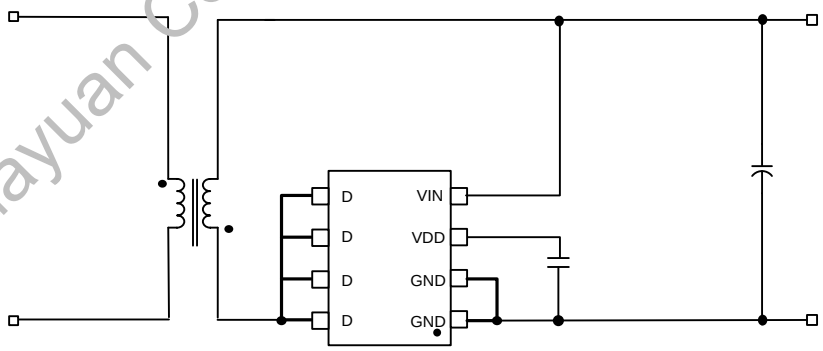



Fig 1.Typical Application Diagram Option Table

**SOP8(Top view)**

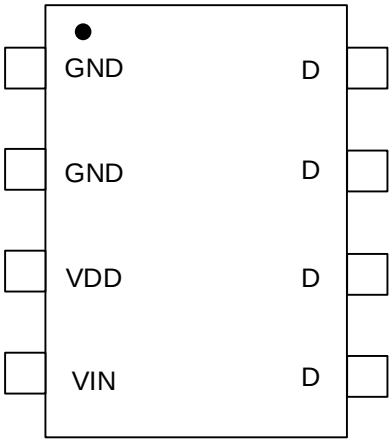



Fig 2.Package Diagram

| Pin | Name | Description |
|---|---|---|
| 1, 2 | GND | Chip ground and internal NMOS source pin” |
| 3 | VDD | IC bias pin. VDD is the supply of the HYC9012. A typical 1uF to 2.2uF X7R bias capacitor is recommended to be designed in applications |
| 4 | VIN | HV bias input pin. VIN pin connected to the front stage converter output voltage. |
| 5,6,7,8 | D | Drain. Connect SR MOSFET drain internally. |

## Absolute Maximum Ratings

| Item | Min | Max | Unit |
|---|---|---|---|
| VDD | -0.3 | 9.0 | V |
| VIN | -0.3 | 28.0 | V |
| D | -1.0 | 100 | V |
| $T_J$(Operation junction temperature) | -25 | 150 | ℃ |
| $T_S$(Storage temperature) | -40 | 150 | ℃ |

Note 1: Stresses beyond Absolute Maximum Ratings may cause permanent damage to the device.

## ESD Ratings

| Item | Definition | Value | Unit |
|---|---|---|---|
| Electrostatic Discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001-2017 | ±3500 | V |
| | Charged device model (CDM), per JEDEC specification JESD22-C101 | 500 | V |

## Thermal Specification

| Item | Value | Unit |
|---|---|---|
| $\theta_{JA}$ Junction-to-ambient thermal resistance | 132 | ℃/W |
| $\theta_{JC}$(top) Junction-to-case (top) thermal resistance | 39 | ℃/W |

Note 2: The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$(MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX)- T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

## Electrical Characteristics

VIN= 20V, 25℃ ambient temperature, unless otherwise noted.

| Parameter | Description | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **VIN** | | | | | | |
| VIN_MAX | Maximum VIN Voltage | | | | 25 | V |
| VIN_DBL_ST | VIN Voltage Threshold for Doubler Regulation Start | VIN Rising from 0V to VDD Start to Regulate as 4.8V | 3.0 | | | V |
| **VDD Bias Supply** | | | | | | |
| VDD | VDD Clamp Maximum | VIN Rising from 0V to 20V | | 8.0 | | V |
| VDD_ON | VDD POR Threshold | VDD Rising from 0V to 8V | 3.6 | 4.2 | 4.4 | V |
| VDD_OFF | VDD OFF Threshold<br>IC Shuts Down | VDD Falling from 8V to 0V | 2.5 | 3.0 | 3.5 | V |
| VDD_ON_HYS | VDD POR Threshold Hysteresis | | | 0.70 | | V |
| VDD_REG | VDD Doubler Regulation | VIN Rising from 0V to 25V | 4.0 | 4.8 | | V |
| I_DD_NSW | NO Switching Operating Current | VDD= 8V, No Switching | 0.4 | 0.6 | 0.7 | mA |
| IDD | Operating Current with Switching | VDD= 8V, 65kHz Switching, 4.7nF Equivalent Gate Cap | | 3.6 | | mA |
| I_SD | Shutdown Current | VDD<VDD_OFF | | 20 | | μA |
| **D Pin to GND Pin (Drain to Source)** | | | | | | |
| V_DS_ON | Switch ON Threshold of (VD-GND) | VDD= 8V, (VD-GND) falling | -175 | -200 | -225 | mV |
| V_DS_OFF | Switch Off Threshold of (VD-GND) | VDD= 8V, (VD-GND) rising | -17.5 | -20 | -22.5 | mV |
| V_DS_REG | Gate Pre-off Threshold of (VD-GND) | | -45 | -53 | -60 | mV |

| | | | | | | |
|---|---|---|---|---|---|---|
| V_ST | Shoot Through Protection Threshold of (VD-GND) | VDD=8.0 | | 600 | | mV |
| **Power Switch** | | | | | | |
| $V_{DS\_BR}$ | Drain to Source Break Down Voltage | VIN=0V, VDD=0V | 100 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{GS}$=0V, $V_{DS}$=100V, Tj=25°C | | 0.1 | 1 | μA |
| | | VIN=0V, VDD=0V, $V_{DS}$=100V, Tj=125°C | | 10 | 100 | μA |
| $R_{DS\_ON}$ | Switch on State Resistance | $V_{GS}$=10V, $I_D$=20A | | 9 | | mΩ |
| $I_D$ | Continuous Drain Current | $V_{GS}$=10V, Tc=25°C | | | 40 | A |
| $I_{D\_P}$ | Pulse Drain Current | $V_{GS}$=10V, Tc=25°C | | | 160 | A |
| $E_{AS}$ | Avalanche energy, single pulse | $I_D$=21.5 A, L=0.5mH | | 146 | | mJ |
| **Power Switch Dynamic Characteristics** | | | | | | |
| $C_{OSS}$ | Output Capacitance | $V_{GS}$=0V<br>$V_{DS}$=50V<br>fs=1MHz | | 324 | | pF |
| **Source Drain Diode Characteristics** | | | | | | |
| $I_F$ | Diode Continuous Current | Tc=25°C | | | 40 | A |
| $I_{F\_P}$ | Diode Pulse Current | Tc=25°C | | | 160 | A |
| $V_F$ | Diode Forward Voltage | $V_{GS}$=0 V, $I_F$=20 A, Tj=25 C | | 0.9 | 1.2 | V |
| $T_{RR}$ | Reverse Recovery Time | VD=40 V, $V_{GS}$=10V, $I_F$=10A, dI/dt=100 A/μs | | 60 | | ns |
| $Q_{RR}$ | Reverse Recovery Charge | | | 97 | | nC |

# IC Function Diagram

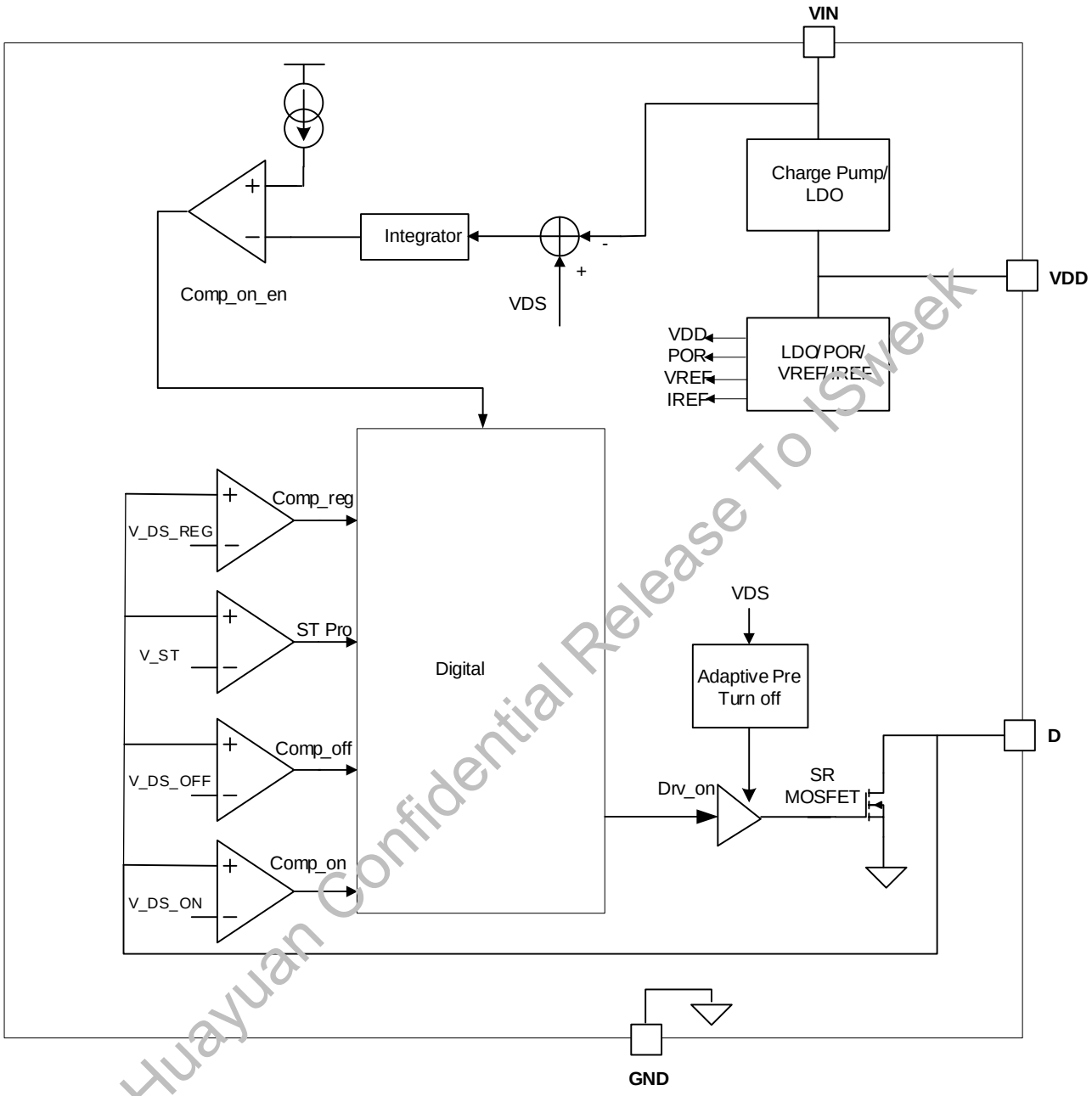





Fig 3.HYC9012 Function Block Diagram

## Detail Function Description

HYC9012 is a digital control synchronous rectifier controller integrated together with SR MOSFET. It detects VDS of SR MOSFET to control the turning ON/OFF timing. When SR MOSFET VDS is below V_VDS_ON threshold, SR MOSFET is turned on. When SR MOSFET VDS is higher than V_VDS_OFF threshold, SR MOSFET is turned off. The adaptive control scheme of pre-turn off minimizes the turn off transition of the SR MOSFET.

The adaptive gate pre-turn off scheme improves the EMI due to soft SR MOSFET turning off. It minimizes switching loss due to less conduction overlap between primary MOSFET and SR MOSFET under CCM. A fixed minimum turning on time and turning off time improve the immunity to noise and prevent SR MOSFET mis-triggering due to the current ring noise coupling to VDS signal. VDD internal charge pump and clamp circuit make HYC9012 operate reliably under wide range of VIN. VIN connects with DC output directly.

### VDD Bias

The VDD bias diagram is shown in Fig 4. HYC9012 is powered from VIN and generates the power supply for the internal circuits at VDD. HYC9012 implements the charge pump circuit to regulate the VDD voltage at 4.8V at the VIN ranges of 3.0V to 5V. It implements the voltage follower at the VIN range of 5V to 8V. VDD is clamped at 8V in HYC9012if the VIN is above 8V. When VDD reaches VDD_ON threshold, HYC9012 consumes normal operating current. When VDD is decreased as low as VDD_OFF, HYC9012 shuts down.

A typical 1uF to 2.2uF X7R capacitor is recommend between VDD and GND with short trace.

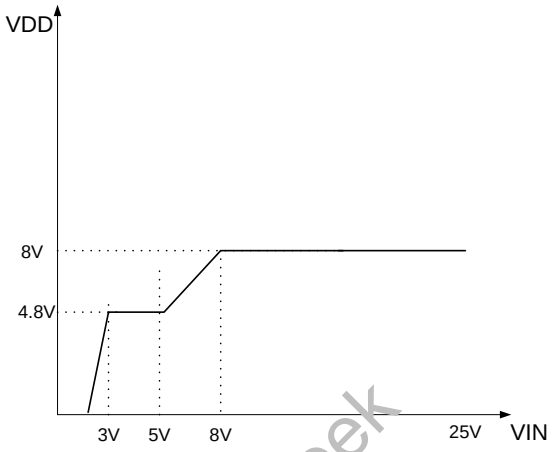



Fig 4.VIN and VDD Bias Diagram

### SR MOSFET Control Scheme

*SR MOSFET Turning On*

The voltage drop across the drain to source of SR MOSFET is sensed from drain of SR MOSFET reference to GND. When primary MOSFET turns off, the drain voltage of SR MOSFET sharply drops from positive to negative. This transition duration is tens of nanoseconds depending on different applications. The threshold to determine the SR MOSFET turning on is V_DS_ON. When drain signal is below V_DS_ON during falling transition, HYC9012 turns on SR MOSFET with minimum turning on delay. To minimize turning on transition time and turning on delay is one of the important factors to reduce the switching loss of flyback converter. After SR MOSFET turns on, a minimum turning on time window is designed in HYC9012 to mask the mis-trigger turning off scenario due to the current ring right after the SR MOSFET turns on.

*SR MOSFET Turning Off*

The voltage on the drain of SR MOSFET continuously senses the drain-source voltage after SR MOSFET turns on. The voltage signal applies to drain of SR MOSFET is a negative $R_{DS\_ON}$ voltage drop during the SR MOSFET conduction. To minimize the conduction loss of SR MOSFET, the voltage drops across the VDS should be minimized.

HYC9012 regulates SR MOSFET gate voltage when VDS sign across the threshold V_DS_REG. Once VDS voltage across V_DS_REG, internal gate drive circuit continuously drops gate signal voltage and maintain VDS voltage as V_DS_REG, as shown in Fig 5. This scheme prevents SR MOSFET from premature turning off. In the meantime, the turn-off transition and delay time of SR MOSFET is minimized by using this pre-turn off scheme.

When the secondary current drops and the VDS voltage signal across the V_DS_OFF threshold, the SR MOSFET turns off. After SR MOSFET turns off, a minimum turning off time window is designed in HYC9012 to mask the mis-trigger turning on scenario due to the current ring right after the SR MOSFET turns off, as shown in Fig 5. When the system operates under CCM, the waveform is shown as in Fig 6. It is noticed that, the pre-turning off time can be very short or totally disappeared under CCM operation.

It is noted that, a fixed turning off blanking timer does not always work well for the entire range of line and load conditions in different applications. A flyback under quasi-resonant (QR) operation, system may operate in DCM under light load condition. In this case, the turning off blanking time should be long enough to avoid DCM ringing causing SR false turning on. On other hand, when the converter operates in QR mode under high input voltage, the primary side MOSFET switching on-time is short, and the minimum off-time may cut into the conduction of the SR. In this case, there is an extra conduction loss as the body diode of SR MOSFET conducts if the minimum off-time masks the beginning portion of SR MOSFET turning on.



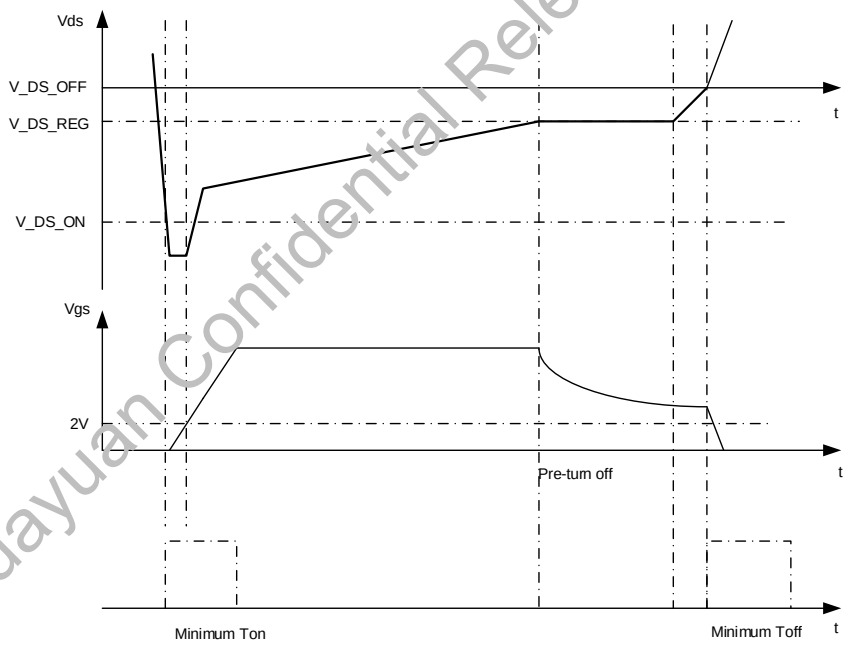



Fig 5.SR MOSFET Turning ON/OFF Diagram under DCM

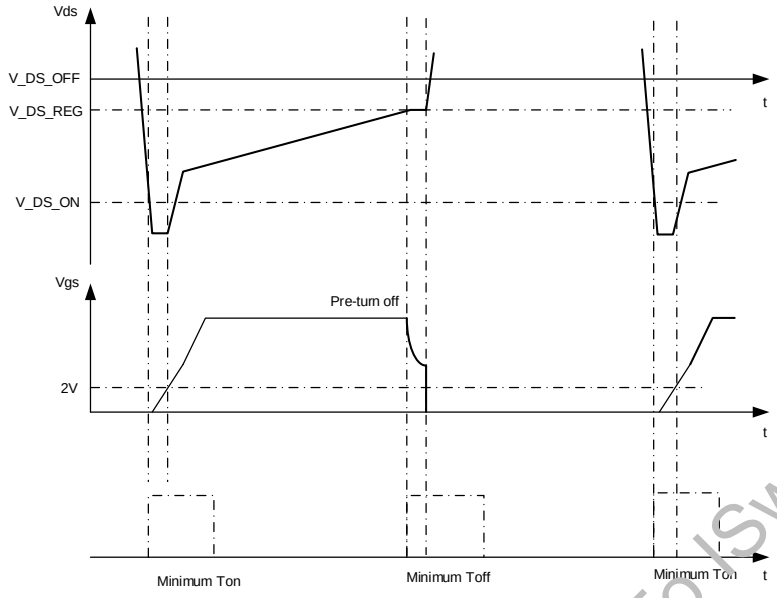



Fig 6.SR MOSFET Turning ON/OFF Diagram under CCM

### Shoot Through Protection (STP)

In any cases, if primary switch turns on while SR MOSFET is still on, the current on the secondary side conducts from drain to source of SR MOSFET. This current direction is reversed from the normal secondary current that charges output cap. This current discharges output DC cap and rises sharply as it is a shoot through current.

HYC9012 designs an internal shoot through protection by a fast comparator. The threshold of the STP is 600mV. Once the voltage across VDS of SR MOSFET triggers the shoot through protection threshold, V_ST, the SR controller shuts down the SR MOSFET immediately. This STP function effectively protects primary MOSFET and SR MOSFET from blowing up.

## Application

HYC9012 is designed for high performance AC to DC offline solution. It is designed to perform as diode emulator circuit. HYC9012 can achieve high efficiency, low EMI, low BOM and high reliability application system. The typical AC/DC offline application diagrams that HYC9012is connected at low side on the secondary are shown in Fig 7. In these application diagrams, the primary controller is HY1602.

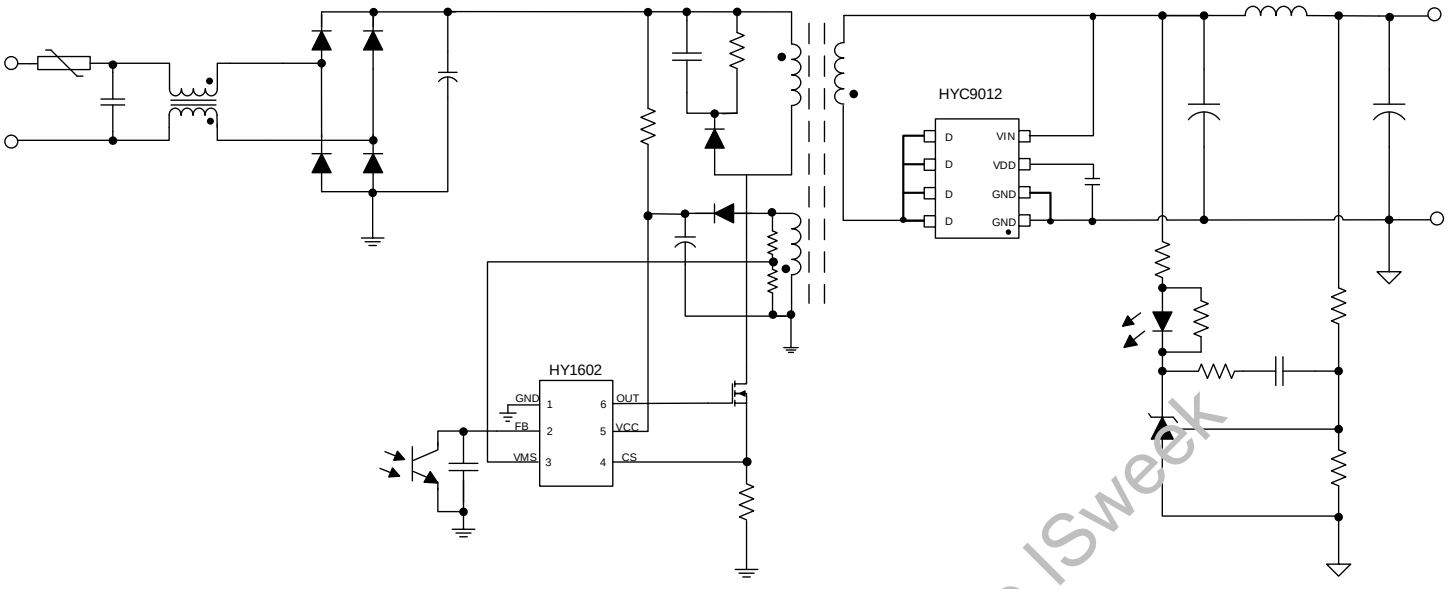


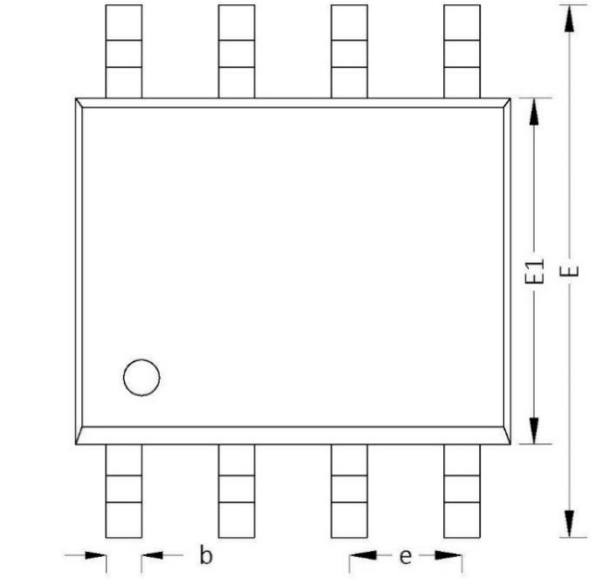

Fig 7.Application Diagram of HYC9012

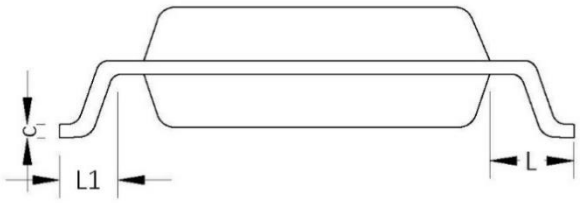
## PCB Layout

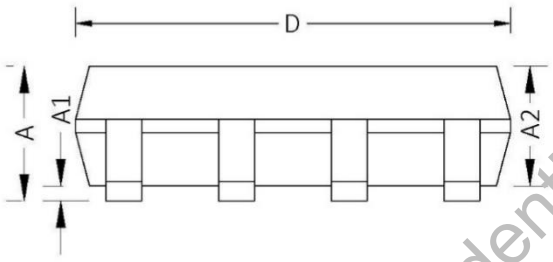
It is recommended to pay attention on the layout of HYC9012 in AC/DC offline applications in order to achieve reliable operation and high performance of the flyback converters.

1) VDD bypass cap: the low ESR ceramic capacitor is required to be as close as possible to VDD and GND pins on PCB layout.
2) GND pins must be connected together by thick PCB trace. In the layout, GND pin is recommended to connect the negative polarity of output electrolytic cap with thick metal trace as close as possible.
3) D pin is connected with drain of SR MOSFET internally. In the layout, D pin is recommended to connect the transformer winding with thick metal trace as close as possible.

# SOP8 Package

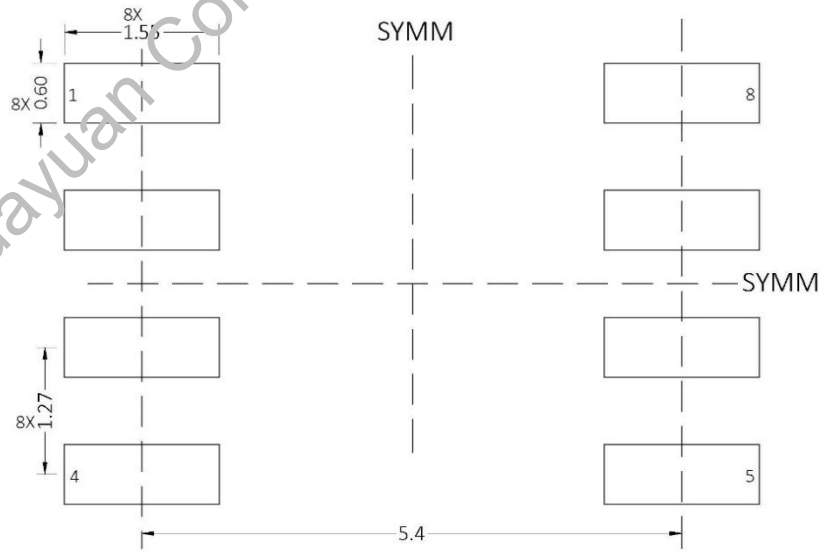



| SOP8 COMMON DIMENSIOS(millimeter) | | | |
|---|---|---|---|
| SYMBOL | MIN | NOM | MAX |
| A | - | - | 1.75 |
| A1 | 0.10 | - | 0.25 |
| A2 | 1.25 | - | 1.65 |
| b | 0.32 | - | 0.50 |
| c | 0.15 | 0.20 | 0.25 |
| D | 4.70 | 4.90 | 5.00 |
| E | 5.80 | 6.00 | 6.20 |
| E1 | 3.70 | 3.90 | 4.00 |
| e | 1.27REF | | |
| L1 | 0.40 | - | 0.80 |
| L | 1.00 | 1.05 | 1.10 |

DIMNSIONS:MILLIMETERS




**Recommended Land Pattern**

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