

NTP8808

**High Performance, High Fidelity Power
Driver Integrated Full Digital Audio Amplifier**

**Datasheet
Preliminary ver. 0.3**



General Description

The NTP8808 is a single chip full digital audio amplifier including power stages for stereo amplifier systems. NTP8808 is integrated with versatile digital audio signal processing functions, high-performance, high-fidelity fully digital PWM modulator and two high-power full-bridge MOSFET power stages.

The NTP8808 receives digital serial audio data with sampling frequencies from 8kHz through 192kHz. It delivers 2 x 25 watts in the stereo mode without a heat sink.

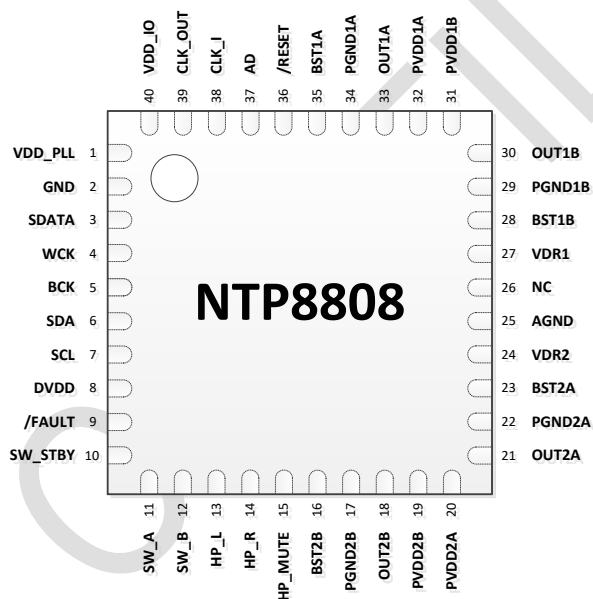
The NTP8808 has a mixer and Bi-Quad filters which can be used to implement essential audio signal processing functions like compensation of a loud speaker response and parametric equalization.

All the functions of the NTP8808 can be controlled by internal register values via I²C host interface bus.

Features

- 2 CH Stereo (25W x 2 BTL @24V, 6Ω)
- 2.1CH (10W x 2 + 25W @24V, 6Ω)
- SDATA Generator (I²S output)
- Wide Operating Supply Voltage Range (7V to 28V)
- Floating Point Operation
- 25 Programmable Bi-Quad Filters
 - ✓ Speaker Compensation
 - ✓ LPF, HPF
 - ✓ Parametric Equalizer
- 100dB Dynamic Range
- 2 Band Dynamic Range Control
- Protection Circuit
 - ✓ OCP(Over Current Protection)
 - ✓ OTP(Over Temperature Protection)
 - ✓ UVP(Under Voltage Protection)
- High Efficiency
- Asynchronous Sample Rate Conversion
- DC cut filter

Package



(40 pin SAW QFN 6mm x 6mm Package)

Applications

- PDP TV or LCD TV
- Docking Station
- Mini-Component Audio Solution

Ordering Information

| Product ID | Package Type | Pin | Size |
|------------|--------------|-----|---------|
| NTP8808 | SAW QFN | 40 | 6 x 6mm |

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Disclaimer

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1. BLOCK DIAGRAM

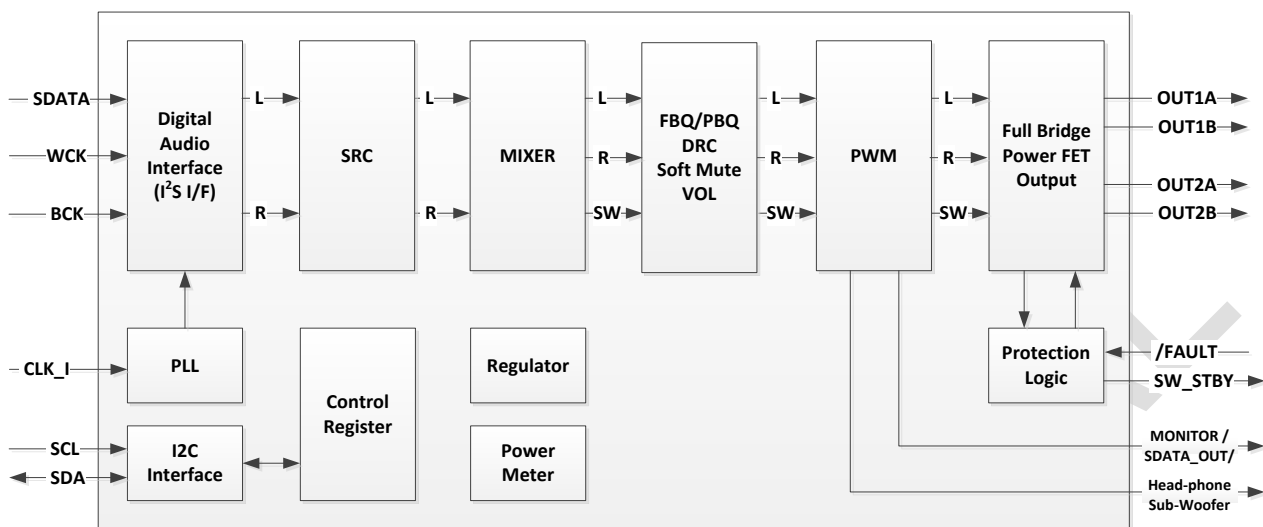


Figure 1. NTP8808 Block Diagram

2. PIN ASSIGNMENTS

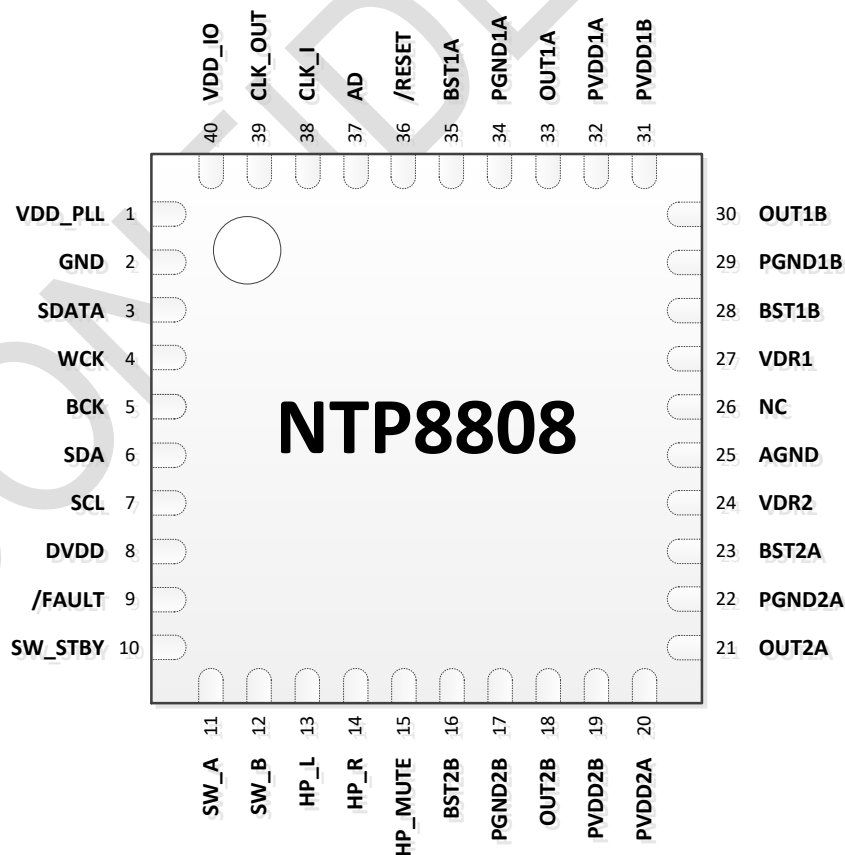


Figure 2. NTP8808 Pin Assignments

3. PIN DESCRIPTIONS

| PIN | NAME | TYPE | DESCRIPTION |
|-----|--------------------|------|---|
| 1 | VDD_PLL | P | Regulator output for PLL digital block, 1.2V |
| 2 | GND | P | This pin should be connected to Ground |
| 3 | SDATA | I | I ² S serial data input |
| 4 | WCK | I | I ² S word clock |
| 5 | BCK | I | I ² S bit clock |
| 6 | SDA | I/O | I ² C data |
| 7 | SCL | I | I ² C clock |
| 8 | DVDD | P | Regulator output for Core block, 1.2V |
| 9 | /FAULT | I | Active low to reset internal power stage, Pull-up |
| 10 | SW_STBY | O | External power device standby control |
| 11 | SW_A/ MONITOR_0 | O | Sub-Woofer_A/Monitoring signal out from processor block |
| 12 | SW_B/ MONITOR_1 | O | Sub-Woofer_B/Monitoring signal out from processor block |
| 13 | HP_L | O | Left audio channel Headphone signal |
| 14 | HP_R | O | Right audio channel Headphone signal |
| 15 | HP_MUTE | O | External Headphone mute signal |
| 16 | BST2B | P | Bootstrap supply, external capacitor to OUT2B is required |
| 17 | PGND2B | P | Ground |
| 18 | OUT2B | O | Power stage PWM output 2B |
| 19 | PVDD2B | P | Power supply for PWM Power stage 2B |
| 20 | PVDD2A | P | Power supply for PWM Power stage 2A |
| 21 | OUT2A | O | Power stage PWM output 2A |
| 22 | PGND2A | P | Ground |
| 23 | BST2A | P | Bootstrap supply, external capacitor to OUT2A is required |
| 24 | VDR2 | P | Gate drive voltage regulator decoupling pin, capacitor to GND is required |
| 25 | AGND | P | Ground |
| 26 | NC | - | No connection |
| 27 | VDR1 | P | Gate drive voltage regulator decoupling pin, capacitor to GND is required |
| 28 | BST1B | P | Bootstrap supply, external capacitor to OUT1B is required |
| 29 | PGND1B | P | Ground |
| 30 | OUT1B | O | Power stage PWM output 1B |
| 31 | PVDD1B | P | Power supply for PWM Power stage 1B |
| 32 | PVDD1A | P | Power supply for PWM Power stage 1A |
| 33 | OUT1A | O | Power stage PWM output 1A |
| 34 | PGND1A | P | Ground |
| 35 | BST1A | P | Bootstrap supply, external capacitor to OUT1A is required |
| 36 | /RESET | I | Active low to reset NTP8808, Schmitt trigger input |
| 37 | AD | I | I ² C device address selection |
| 38 | CLK_I | I | System master clock input |
| 39 | CLK_OUT | O | System master clock output |
| 40 | VDD_IO | P | Power supply for digital interface I/O, 3.3V |
| - | Thermal Pad | P | This pad should be connected to Ground |

P = Power Supply or Ground, I = Input, O = Output, I/O = Input / Output

Table 1. NTP8808 Pin Description

4. CHARACTERISTICS AND SPECIFICATIONS

4.1. Absolute Maximum Ratings

| Parameter | Reference | Rating | Unit |
|----------------------|----------------|---------------|------|
| DVDD voltage | DGND | -0.3 ~ 1.5 | V |
| VDD_IO voltage | GND_IO | -0.3 ~ 5.25 | V |
| Logic input voltage | GND | -0.3 ~ 5.25 | V |
| Logic output voltage | GND | -0.3 ~ 5.25 | V |
| PVDDXX voltage | PGNDXX | 30 | V |
| OUTXX voltage | PGNDXX | -0.3 ~ PVDDXX | V |
| BSTXX voltage | PGNDXX | 36.0 | V |
| VDRX voltage | PGNDXX | -0.3 ~ 6.0 | V |
| Junction temperature | T _j | 150 | °C |

4.2. Recommended Operating Conditions

| Parameter | Reference | Min | Typ | Max | Unit |
|-------------------------------|------------------|-----|-----|-----|------|
| VDD_IO voltage | GND_IO | 3.0 | 3.3 | 3.6 | V |
| PVDDXX voltage | PGNDXX | 7 | | 28 | V |
| VDRX voltage | PGNDXX | | 5.1 | | V |
| Ambient operating temperature | T _{AMB} | -25 | | 85 | °C |

4.3. DC Electrical Characteristics

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|--|-------------------|--|------|-----|------|------|
| Logic Block (VDD_IO=3.3V, T _A =+25°C, unless otherwise specified.) | | | | | | |
| Input High voltage | V _{IH} | - | 2.0 | | | V |
| Input Low voltage | V _{IL} | - | -0.5 | | 0.8 | V |
| Schmitt trig. Low to High threshold point | V _{T+} | - | 2 | | 3.6 | V |
| Schmitt trig. High to Low threshold point | V _{T-} | - | -0.5 | | 0.8 | V |
| Input current | I _I | V _{IN} =V _{IL} MAX, DVDD=MIN | -50 | | | uA |
| | | V _{IN} =V _{IH} MIN, DVDD=MIN | | | 50 | uA |
| Input leakage current | I _L | V _{IN} =VSS, DVDD=MIN | -10 | | 10 | uA |
| Output Low voltage | V _{OL} | I _{OL} = -4mA | 0 | | 0.4 | V |
| Output High voltage | V _{OH} | I _{OH} = 4mA | 2.4 | | 3.6 | V |
| LDO output voltage | V _{LDO} | DVDD | 1.08 | | 1.32 | V |
| Power Driver Block (PVDDXX=20V, T _A =+25°C, unless otherwise specified.) | | | | | | |
| Current consumption | I _{CC} | VDD_IO=3.3V, No Input, No Load | | 30 | | mA |
| | I _{PVDD} | PVDD=24V, No Input, 8 Ω Load with 10uH | | 95 | | |
| Peak current limit | OCP | - | 5.0 | 6.5 | 9.0 | A |
| Thermal shutdown temperature | OTP | - | 140 | 150 | 160 | °C |
| Under voltage protection limit | UVP | - | 4.75 | 5.0 | | V |

4.4. PLL Input Parameters and External Filter Components

| Parameter | Min | Typ | Max | Unit |
|-----------------------------------|-------|-----|--------|----------|
| MCLK frequency range | 2.048 | | 49.152 | MHz |
| MCLK duty cycle | 20 | 50 | 80 | % |
| Rise/fall time for MCLK | | | 5 | ns |
| MCLK square wave jitter | | | 0.1 | UI |
| External PLL filter capacitor C10 | | 220 | | nF |
| External PLL filter capacitor C11 | | 22 | | nF |
| External PLL filter resistor R13 | | 220 | | Ω |

4.5. Performance Specification

| Parameter | Condition | Min | Typ | Max | Unit |
|----------------------|--|-----|-----|-----|---------|
| SNR | AES17, A-weighting filter | | 95 | 100 | dB |
| THD+N | 1W, 1kHz | | 0.1 | | % |
| P _{OUT} | Peak output power | | 25 | | W |
| Cross talk | | | 67 | | dB |
| Output noise voltage | P _{VDD} =24V | | 500 | | μ V |
| Efficiency | P _{VDD} =12V, P _{OUT} =15W @ 6 Ω , THD 1% | | 90 | | % |
| PWM frequency | | | 384 | | KHz |

4.5. Switching Characteristics – I²C Control

| Parameter | Symbol | Condition | Min | Max | Unit |
|------------------------------------|--------------------|-----------|------|-----|------|
| I²C Control Port | | | | | |
| SCL clock frequency | F _{scl} | | - | 400 | kHz |
| Hold time for START condition | T _{hdsta} | | 600 | - | ns |
| Low period of the SCL clock | T _{low} | | 1300 | - | ns |
| High period of the SCL clock | T _{high} | | 600 | - | ns |
| Rise time of SDA and SCL signals | T _{rise} | | - | 300 | ns |
| Fall time of SDA and SCL signals | T _{fall} | | - | 300 | ns |
| Setup time for STOP condition | T _{susto} | | 600 | - | ns |

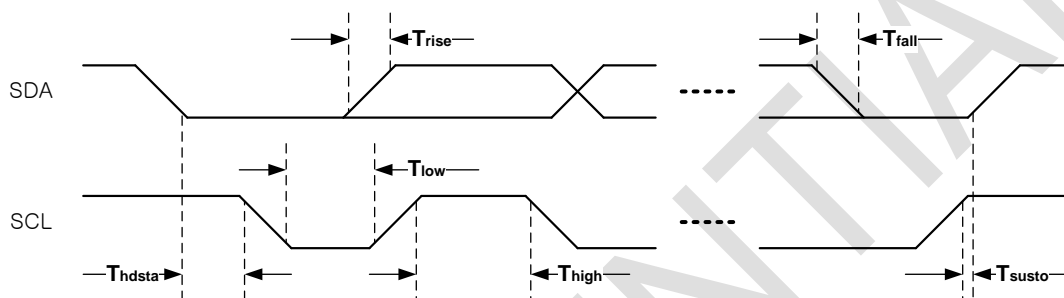


Figure 3. I²C Mode Timing

4.6. Switching Characteristics – Audio Interface

| Parameters | Symbol | Min | Max | Unit |
|---|--|-----|-----|------|
| BCK high time | t _{bh} | 20 | - | ns |
| BCK low time | t _{bl} | 20 | - | ns |
| SDATA setup time before BCK rising edge | t _{ds} | 10 | - | ns |
| SDATA hold time after BCK rising edge | t _{dh} | 10 | - | ns |
| WCK setup time before BCK rising edge | t _{ws} | 20 | - | ns |
| BCK rising edge before WCK edge | t _{wh} | 20 | - | ns |
| BCK falling edge before WCK edge | t _{wl} | -20 | 20 | ns |
| Rising/Falling time for BCK/WCK | t _{br} /t _{bf} /t _{wrf} | - | 50 | ns |

※ Schmitt trigger characteristics (V_{SIH} Min = 1.85V, V_{SIH} Max = 0.9V)

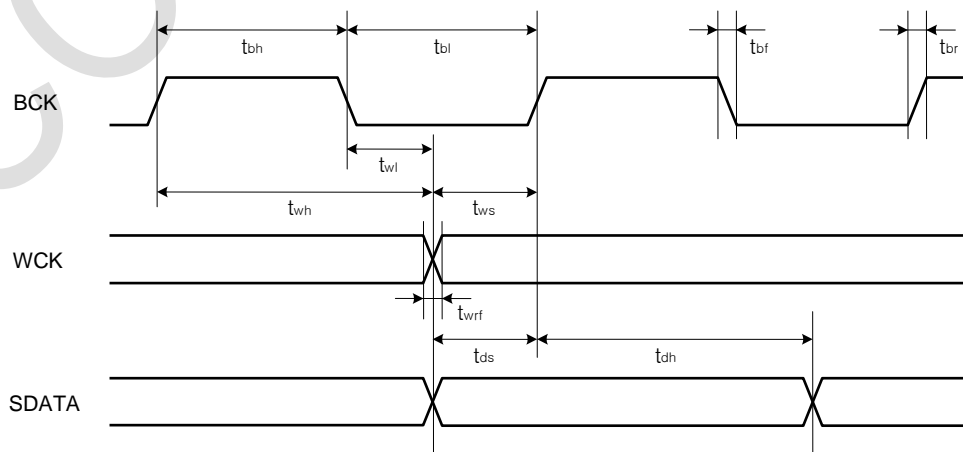


Figure 4. Audio Interface Timing

5. I²C BUS OF NTP8808

The NTP8808 uses an industry standard Inter IC Control (I²C) bus to communicate with host IC. A host IC can write or read internal registers of the NTP8808 via the I²C bus.

5.1. General Description of I²C Bus

The I²C bus uses two signal lines – a serial clock line (SCL) and a serial data line (SDA). Because the SDA line is open-drain type port, both the NTP8808 and a host IC can only drive these pins low or leave them open.

In I²C bus, a master device means the device which generates serial clock on the SCL. A slave device means the device which receives serial clock. There can be many master and slave devices on an I²C bus. But, when one master device works on the bus, the other master devices should not generate signal on the lines. These unexpected interrupts can make other slave devices to fail to communicate with the mater device.

The NTP8808 supports only slave mode of I²C bus. So, the NTP8808 always receives serial clock from a host IC. The slave mode is enough to write/read data to/from the NTP8808.

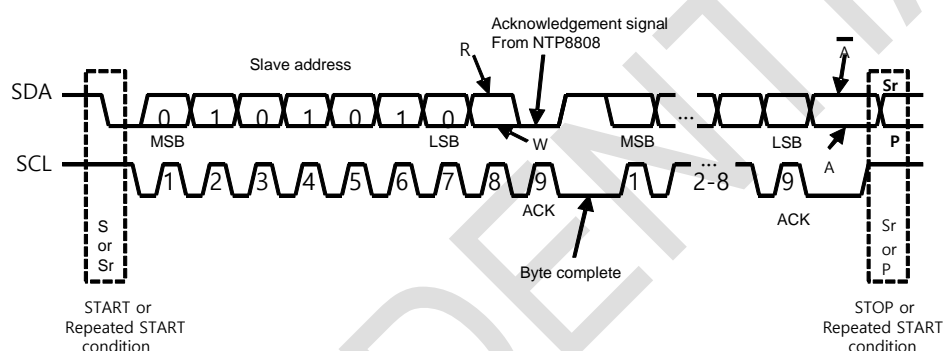


Figure 5. Basic Signaling Elements of I²C Bus

If there are no communication on I²C bus, lines must keep in high state. I²C bus begins communication with the start condition and ends communication with the stop condition. The start condition can be generated by changing the SDA state high to low, during the SCL state remains in high. The stop condition can be generated by changing the SDA state low to high during the SCL remains in high state. Be aware that the stop condition always reset the internal status of I²C bus control logic. Except these two conditions, the SDA may not change during the SCL in high state. Otherwise, abnormal start or stop condition will be generated.

I²C bus transfers the MSB of a byte on 1st data slot and the LSB of a byte on 8th data slot. I²C bus checks success or fail of transfer on every 1 byte transfer. The device which found an expected data on SDA must generate acknowledgement (keep low on SDA) on 9th clock. If there is no acknowledgement on 9th clock, the device which generated a data on SDA may stop transfer. The NTP8808 will generate acknowledgement for every successful data transfer of 1 byte in write mode. But, in read mode, because data is generated by the NTP8808, the NTP8808 will not generate an acknowledgement. In this case, on the contrary, the NTP8808 will check SDA state on 9th clock that the master device received a read data properly.

Last 8th bit of the 1st byte is used to indicate whether the master device want to write or read data.

5.1.1. Writing Operation

When last 8th bit of the 1st byte is set to low state, the writing operation of bus begins. The NTP8808 supports 3 kind of writing operations which presented on **Figure 6**

The type presented on **Figure 6-(a)** is single byte write operation. “Sub address” on 2nd byte means the internal register address of the NTP8808. The “Data” on 3rd byte will be written into the internal register address on “Sub address”. If stop condition is not generated, writing “data” on specific “sub address” can be repeated like **Figure 6-(b)**. “Data #n” will be written on “sub address #n”.

The type presented on **Figure 6-(c)** is burst byte write operation under address auto increment mode. The AIF is the address Auto Increment Flag which is 1st bit of 2nd byte of I²C packet. On SDA, if AIF is set to high state, the NTP8808 starts auto incrementing the address with respect to given “sub address” and host send write data continuously over SDA. In AIF mode, access to the register addresses 0x3B~0x49, 0x4F and 0x5E are automatically skipped.

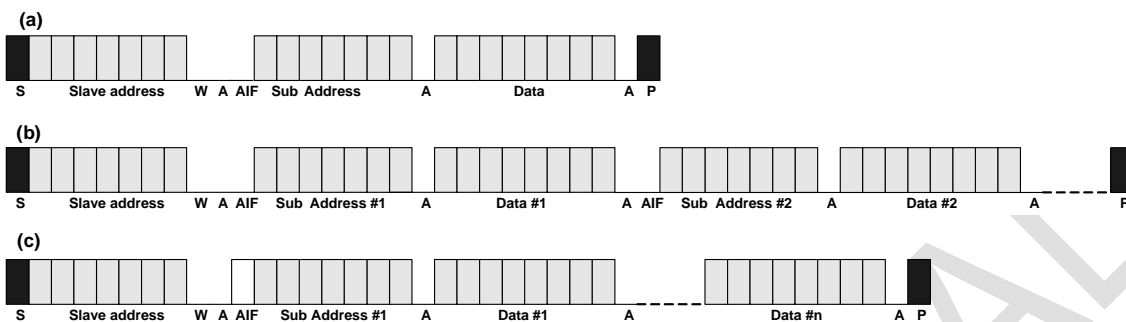


Figure 6. Single Byte Write Mode Sequence

Figure 7-(a), **Figure 7-(b)**, and **Figure 7-(c)** represent 4 byte writing operations. Coefficient Mode Register address 0x00~0x6B are used to configure Bi-Quad filter coefficients, Low Shelf BQ filter coefficients and DRC clip down gain. The data size of these coefficients and gains is 4 byte for each. The difference between 4byte writing operation and single byte writing operation is only the size of transferring data. So, after sending “Sub address”, 4 sequential bytes must be transferred from the MSB(most significant byte) to the LSB(least significant byte) sequence.

The type presented on **Figure 7-(c)** is quad byte write operation under address auto increment mode, AIF function. Please compare the data transfer size between **Figure 6** and **Figure 7**.

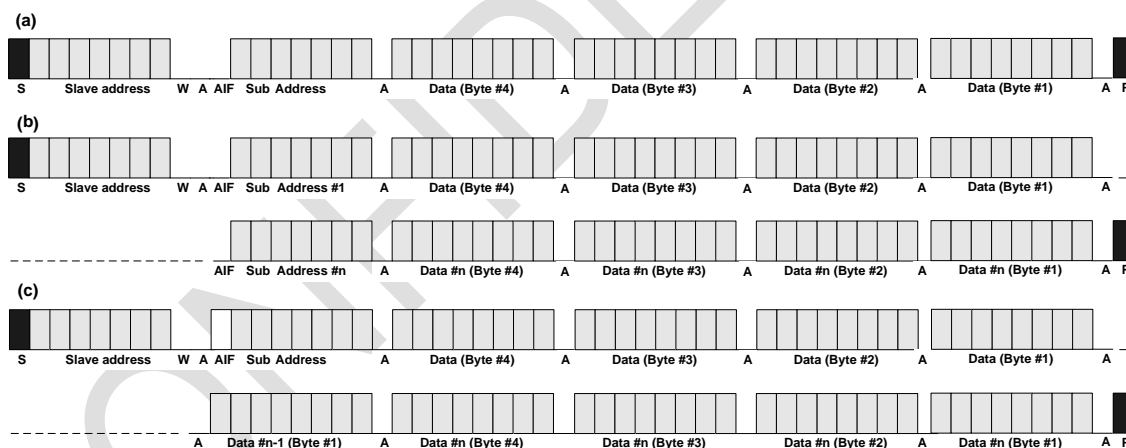


Figure 7. Quad Byte Write Mode Sequence

In write operation, the register 0x7E value needs to be set first for performing the configuration of the registers belong to all channels. The 0x7E register also support to configuring byte writes operation and word i.e. 4 byte writes operation.

If 0x7E register is configure to 0x00, it support byte write operation and for word i.e. 4 byte write operation for each channel it needs to configure as 0x01 for channel 1, 0x02 for channel 2, 0x04 for channel 3 and 0x08 for PEQ coefficient. Also to configure channel1 and channel2 with the same values, the 0x7E register needs to configure as 0x03. So the same values get sets for both the channel with only one write operation.

The ROM BQ addresses from 0x00 to 0x3B and from 0x41 to 0x63 are used for the Bi-Quad filter coefficients in the coefficient mode. Each Bi-Quad filter uses 5 coefficients. Any unexpected coefficient value changes on any part of 5 coefficients can generate unstable Bi-Quad filter response. For example, if only one of 5 coefficients for a Bi-quad filter is changed and downloaded, its combined 5-

coefficient set can have unstable operation while old and new coefficients are mixed together. Therefore to prevent this kind of problem, the NTP8808 writes coefficients to coefficient registers only when the last 5th coefficients of each Bi-Quad filter are downloaded, which means all of 5 coefficients are fully ready. Please refer to 9.1 for more detailed operation.

5.1.2. Reading Operation

Figure 8-(a) represents single byte reading operation from the NTP8808. To read data from the NTP8808, generate start condition to start transfer. After then, send “slave address” with write mode flag and send the register address(sub address). By regenerating start condition (Sr) again and transferring “slave address” with read mode flag, reading operation begins. The NTP8808 will generate data on SDA signal synchronizing with serial clocks on the SCL. Because the SDA signal generated from the NTP8808, the master device must generate ACK on 9th slot to confirm that the master received read 1 byte successfully. However, if this is just one byte reading operation, NAK (not acknowledged) signal must be generated. Then stop condition must be generated to end transfer.

When AIF set to high on sub address like **Figure 8-(b)**, data will be read continuously with register addresses which are increased from initial “sub address” for every byte. In continue reading operation, the master must generate ACK signal on every 9th bit of the packet to confirm that master has received 1 byte successfully. Otherwise, reading operation will be terminated.

At the end of AIF reading operation, the NAK should be generated on 9th bit of the last data read to stop the AIF continuous reading operation. Also in reading operation access to the register mention in the “Write Operation’ are skipped.

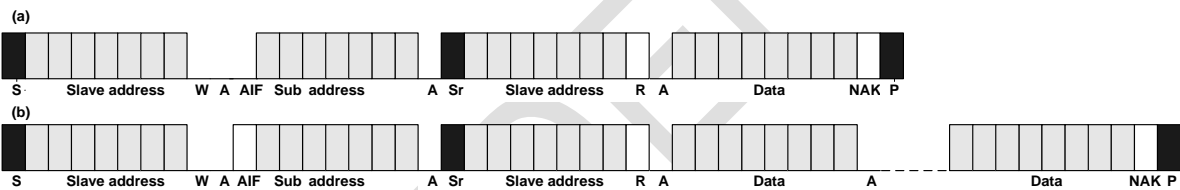


Figure 8. Single Byte Read Mode Sequence

Figure 9 represents quad byte reading operation. The difference between quad byte reading operation and single byte reading operation is only the size of receiving data. So, after sending “Sub address”, 4 sequential bytes must be received from the MSB to the LSB sequence.

The type presented on **Figure 9-(b)** is quad byte read operation under address auto increment mode, AIF function. Please compare the data receive size between **Figure 8** and **Figure 9**.

Before reading operation, the value of register 0x7E should be set first. In case single byte reading operation, set the register 0x7E to “0000”. In case 4 byte reading operation, set the register 0x7E to “0001” for channel1, “0010” for channel2, “0100” for channel3, or “1000” for PEQ coefficient.

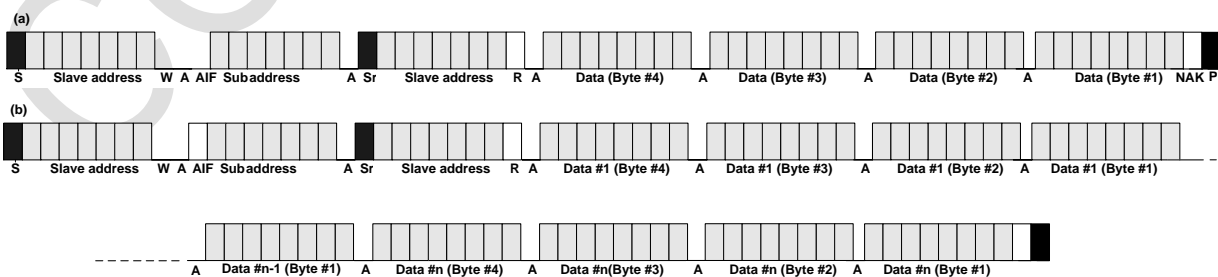


Figure 9. Quad Byte Read Mode Sequence

In read operation, the register 0x7E value needs to be set first for performing the configuration of the registers belong to all channels. The 0x7E register also support to configuring byte reads operation and word i.e. 4 byte reads operation.

If 0x7E register is configure to 0x00, it support byte read operation and for word i.e. 4 byte read operation for each channel it needs to configure as 0x01 for channel 1, 0x02 for channel 2, 0x04 for channel 3 and 0x08 for PEQ. Also to configure channel1 and channel2 with the same values, the 0x7E register needs to configure as 0x03. So the same values get sets for both the channel with only one read operation.

5.2 I²C Glitch Filter

To clean out the threats of noise in today's high-speed-board system, the NTP8808 has a glitch elimination filter on the I²C ports. Glitches in the transmission lines of the I²C port can be safely removed with this function. Please refer to the register 0x39.

5.3. I²C Slave Address

The NTP8808 supports up to four slave address. So, four NTP8808 can be connected to the same MCU at the same time. For multi-chip operation, use the proper I²C slave address according to AD pin and the initial state of SW_A / MONITOR_0 pin as shown in **Table 2**.

| | | SW_A / MONITOR_0 | | |
|----------|-------|------------------|---------------|---------------------------|
| Pin name | Value | Pull-down ('L') | Pull-up ('H') | No pd / pu (default: 'L') |
| AD | 0 | Addr : 0x54 | Addr : 0x58 | Addr : 0x54 |
| | 1 | Addr : 0x56 | Addr : 0x5A | Addr : 0x56 |

Table 2. I²C Slave Address

6. CLOCK, RESET & CONTROL

6.1. System Clock

The internal system clock of the NTP8808 is generated from an external master clock by the on-chip PLL. The NTP8808 supports external master clock frequency from 2.048 MHz to 24.576MHz. For proper operation, the registers for the PLL should be set correctly according to master clock frequency (Address 0x02).

6.2. Timing Sequence 1 (recommend)

For proper power up, initialization and power down of NTP8808, it is recommend to use the following sequence as shown in **Figure 10**.

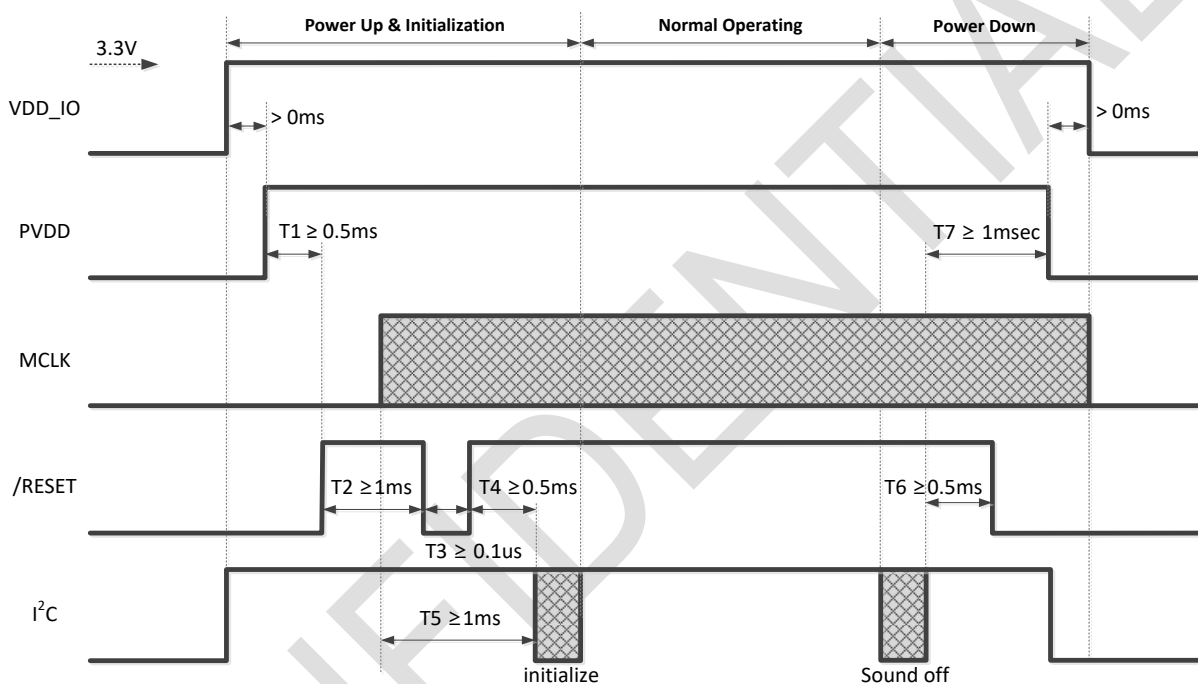


Figure 10. Timing Sequence 1

6.2.1. Power-Up & Initialization Sequence

- 1) Ramp up VDD_IO to at least 3.3V.
- 2) Ramp up PVDD.
- 3) After 0.5msec ($T1 \geq 0.5\text{msec}$), drive /RESET = High, and then wait for at least 1msec ($T2 \geq 1\text{msec}$).
- 4) Hold /RESET Low for at least 0.1usec ($T3 \geq 1\text{usec}$)
- 5) Drive /RESET = High, and then wait for at least 0.5msec for I²C communication ($T4 \geq 0.5\text{msec}$).
- 6) MCLK signal should arrive at least 1msec before I²C initialization sequence ($T5 \geq 1\text{msec}$).
- 7) Execute both amp initialization sequence (e.g. clock, volume, DRC, PEQ setup) and Sound on sequence.

6.2.2. Power-Down Sequence

- 1) When both DC and AC power are off, make sure to execute sound off sequence.
- 2) Switch /RESET to Low after sound off sequence ($T6 \geq 0.5\text{msec}$).
- 3) MCLK and I²C should be Low after sound off sequence ($T7 \geq 0.5\text{msec}$).
- 4) After I²C is Low, ramp down VDD_IO.

6.3. Timing Sequence 2 (reference)

Following figure illustrates another timing sequence, which is conforming to the legacy reset timing.

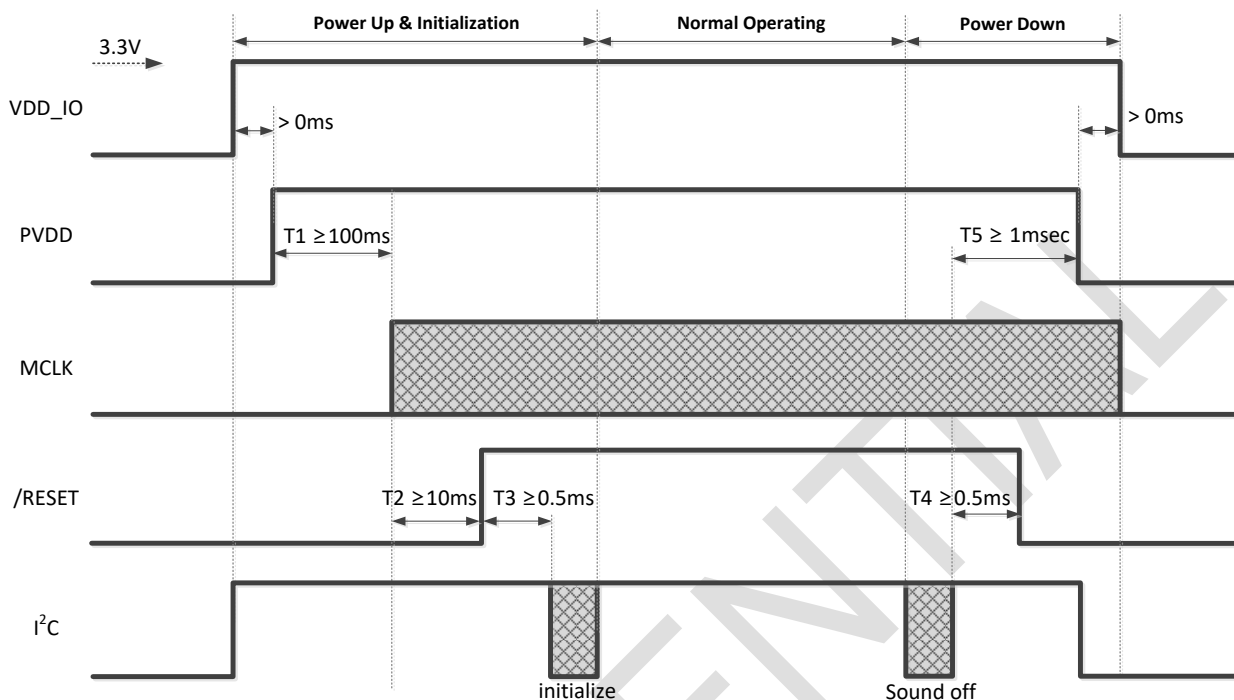


Figure 11. Timing Sequence 2

6.3.1. Power-Up & Initialization Sequence

- 1) Ramp up VDD_IO to at least 3.3V.
- 2) Ramp up PVDD.
- 3) Drive MCLK signal at least 100ms after PVDD ($T1 \geq 100\text{msec}$).
- 4) At least 10ms after MCLK, Drive /RESET = High ($T2 \geq 10\text{msec}$).
- 5) Wait for at least 0.5msec for I²C communication ($T3 \geq 0.5\text{msec}$) and keep the status.
- 6) Execute both amp initialization sequence (e.g. clock, volume, DRC, PEQ setup) and Sound on sequence.

6.3.2. Power-Down Sequence

- 5) When both DC and AC power are off, make sure to execute sound off sequence.
- 6) Switch /RESET to Low at least 0.5 msec after sound off sequence ($T4 \geq 0.5\text{msec}$).
- 7) Ramp down PVDD at least 1 msec after sound off sequence ($T5 \geq 1\text{msec}$).
- 8) After I²C is Low, ramp down VDD_IO.

6.4. Sound On/Off Sequence

For proper sound on/off of NTP8808, use the following sequence as shown in **Figure 12**.

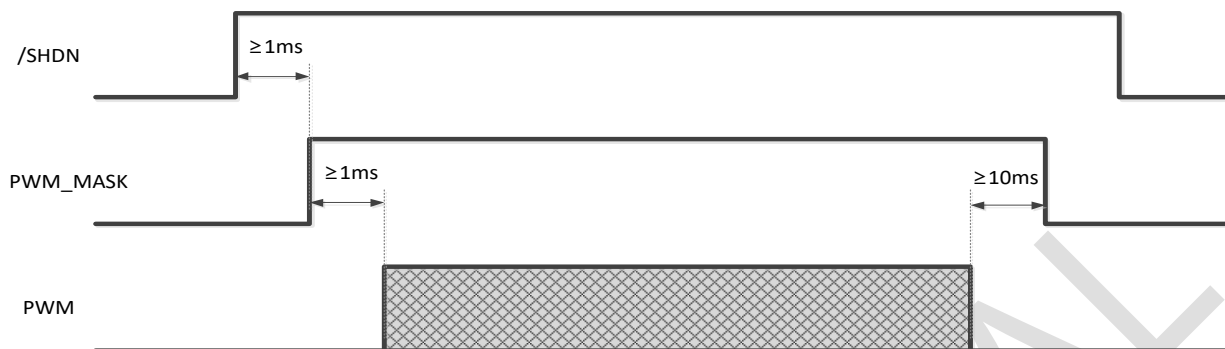


Figure 12. Sound On & Off Sequence

To prevent pop noise when enabling or disabling the amplifier, the following sequences are recommended.

6.4.1. 2-channel Sound On/Off Sequence

A. Sound On Sequence

To turn on the amplifier, first, enable the PWM mask, and then turn on the PWM switching. Finally, apply the soft mute for increasing the output. The register settings are $0x04@0x28$, $0x00@0x27$, and $0x00@0x26$, respectively.

B. Sound Off Sequence

To turn off the amplifier, reverse the sequence of the sound on; that is to say, apply the soft mute for decreasing the output, turn off the PWM switching, and disable the PWM mask. The register settings are $0x07@0x26$, $0x07@0x27$, and $0x06@0x28$, respectively.

6.4.2. 2.1-channel Sound On/Off Sequence

A. Sound On Sequence

Only difference from the 2-channel sound on sequence is that the PWM switching on of the channel 3 should be applied after the channel 1 and 2. Therefore, the sound on sequence for 2.1-channel is as follows: firstly, enable the PWM mask, and, secondly, turn on the PWM switching for channel 1 and 2. Thirdly, turn on the PWM switching for channel 3, and finally, apply the soft mute for increasing the output. The register settings are $0x04@0x28$, $0x04@0x27$, $0x00@0x27$, and $0x00@0x26$, respectively.

B. Sound Off Sequence

The sound off sequence is exactly the same as that in the 2-channel case.

7. AUDIO INPUT

7.1. I²S and Serial Audio Interface

NTP8808 receives audio data through digital audio interface. There are 2 different formats generally used in digital audio interface - the Inter-IC Sound (I²S) Interface and General Serial Audio Interface (GSA). These two interfaces have some common features.

These interfaces use 2 clock lines and 1 data line to transfer audio data. One of these clock lines is the WCK. A period of the WCK is same with sampling period of audio data. This property enables the clock receiving device to synchronize data word-wise transmitting or receiving timing with clock generating device. Another functional aspect of the WCK is indication of current channel. In I²S mode, low state of the WCK indicates 1st channel or left channel, and high state of the WCK means 2nd channel or right channel.

The other clock line is BCK. This clock line is used to synchronize bit-wise timing. The number of clock for one WCK period can be selected on BCKS(Bit Clock Size Select) of register address 0x01.

NTP8808 functions as a slave on the bus. In slave mode, NTP8808 receives WCK and BCK from external source. The data transfer is done via SDATA line. The data being synchronized with the BCK must be loaded on this line. NTP8808 reads data on the rising edge of the BCK. NTP8808 reads data from defined bit range of WCK period. The bit range is selected by the interface type.

The bit range for I²S is predefined. GSA interface can select a bit range with LRJ, MLF and BS of register address 0x01. Please refer to in **Figure 13**.

7.1.1. I²S Glitch Filter

To clean out the threats of noise in today's high-speed-board system, the NTP8808 has a glitch elimination filter on the I²S ports. Glitches in the transmission lines of the I²S port can be safely removed with this function. Please refer to the register 0x61.

7.2. SDATA Generator

The SDATA generator of NTP8808 sends out I²S out signal. In order for SDATA out process to function stably, the falling of BCK should either synchronize or occur ahead of falling or rising of WCK.

Since SDATA generation is synchronous to the input WCK and BCK signals, NTP8808 must be in a slave mode from the point of the I²S signals. Additionally, The I²S transmitter, the master of I²S signals, and NTP8808 should be synchronous. In other words, they have to use the same system clock source to generate SDATA from NTP8808. If the receiver of the generated SDATA does not have an ASRC, it also have to be in the same synchronous clock domain to avoid pop or click noise.

Refer to the register Address 0x5F in the **Appendix A** and refer to the **4.6. Switching Characteristics – Audio Interface**.

7.3. Asynchronous Sample Rate Conversion

NTP8808 provides ASRC(Asynchronous Sample Rate Conversion) for input data sample rate from 8kHz to 192kHz.

ASRC can give seamless data continuity when clock sources of input I²S and MCLK are different. Another benefit of ASRC is audio processing can be done without any change of register settings when there happens an alteration in the input sample rate.

If ASRC is to be used, the LSB of 0x56 register, i.e. BYPASS, should be set as '0'. The default setting of BYPASS in the 0x56 register is '1', which means ASRC is disabled and synchronous conversion is applied.

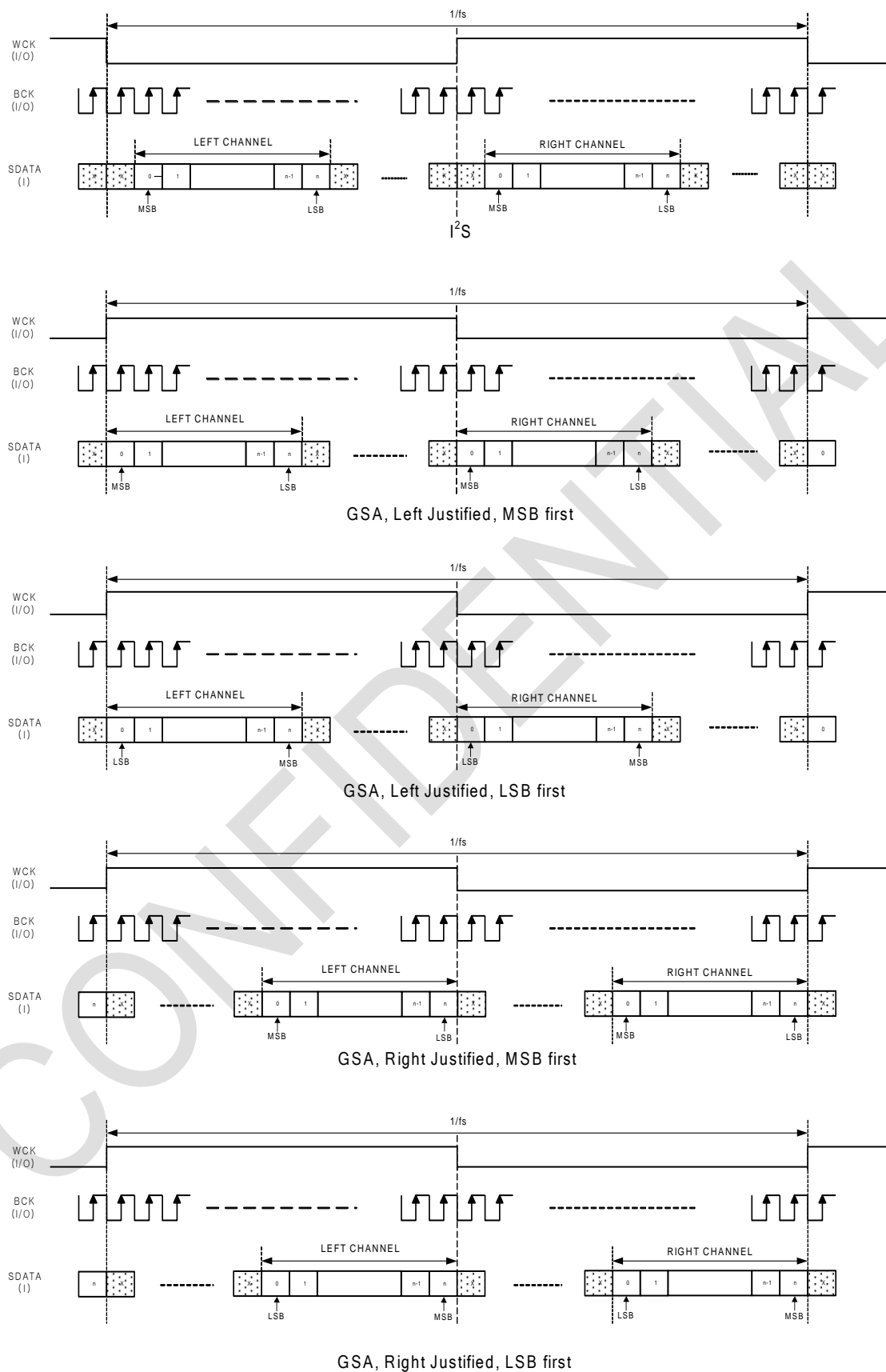


Figure 13. Serial Audio Interface Format

8. MIXER

Channel mixer can be used in lots of application needs like pseudo stereo and etc. User can mix input channels into each output channels with designated gains and polarity. Step size of mixer gain is variable according to the gain level as shown below.

| Volume Range (dB) | Step (dB) |
|-------------------|-----------|
| +18 ~ +6 | 1 |
| +5.5 ~ -5.5 | 0.5 |
| -6 ~ -32 | 1 |
| ≤ 32 | -∞ |

Table 3. Variable Step Mixing Gain

In total, 6 mixing gain coefficients denoted as M[0x03], M[0x04], M[0x05], ... M[0x08] are defined as shown in the equation below. Each Mxx stores volume value in dB scale, and the number values versus gain in dB are shown in the **Appendix B**. There are some places in the mixing matrix that are considered as trivial connections and thus predefined as -∞ dB.

$$[\text{Output Channels}] = [\text{Mixer Matrix}] \times [\text{Input Channels}]$$

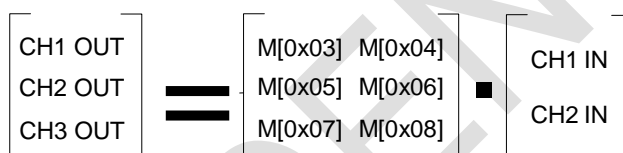


Figure 14. Mixer Matrix

In order to load mixer coefficients into internal memory, send the index value in the gain value table to the register address 0x03~ 0x08.

9. PRE-PROCESSING

9.1. Pre Bi-Quad Filter Chain

NTP8808 has two kinds of Bi-Quad filter chains. One is Pre Bi-Quad filter chain and the other is Post Bi-Quad filter chain for bass management, loud-speaker EQ, etc.

The former is called pre Bi-Quad filter chain and two 2nd order floating point Bi-Quad filters are connected serially to all the three channels. The structure is shown in **Figure 15**.

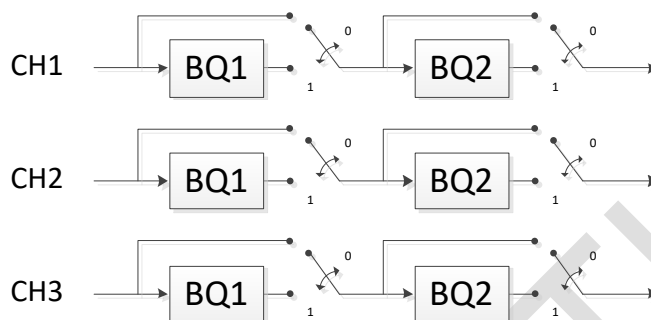


Figure 15. Pre Bi-Quad Filter Structure

Filter coefficients are 32-bit floating point numbers and can be downloaded thru I²C interface. To download the pre Bi-Quad filter coefficients to internal memory of NTP8808, designer should change the flags of register Address 0x7E to 'enable coefficient write' status.

When CH1(or CH2 or CH3) Flag of register Address 0x7E is set to 1, coefficient mode register address 0x00~0x04 designates coefficients of 1st pre Bi-Quad filter chain of channel 1(or channel 2 or channel 3) and indicates b₀, b₁, b₂, a₁, a₂ respectively. coefficient mode register address 0x05~0x09 designates the coefficients of 2nd chain of channel 1(channel 2 or channel 3).

The Bi-Quad filter structure is shown in **Figure 16**.

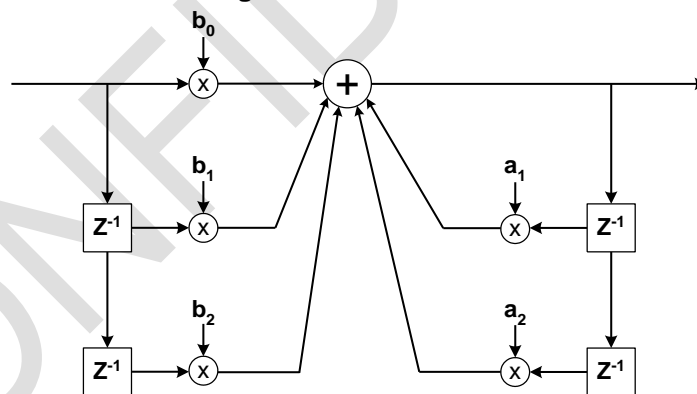


Figure 16. Bi-Quad Filter Structure

9.2. Post Bi-Quad Filter Chain

The post Bi-Quad filter chains of NTP8808 can be used in various purposes - bass management, parametric EQ, loud-speaker EQ, etc. Independent filter design for 1, 2 channels are possible and eight 2nd order floating point parametric filters are linked serially. Filter coefficients are 32-bit floating point numbers and can be downloaded thru I²C interface. To download post Bi-Quad filter coefficients to NTP8808, select download channel by using CH flag in register Address 0x7E first. And then write actual coefficient values, from 0x14 to 0x3B for Ch1&2 Control, from 0x0A to 0x18 for Ch3 control in the coefficient mode register address.

Coefficient mode register address 0x14~0x18 designates 1st chain coefficients and means b0, b1, b2, a1, a2 in sequence. Address 0x19~0x1D designates 2nd chain, and so on. The enable/disable operation of these Bi-Quads can be made by using BQF flag in register Addresses 0x17~0x1B(include Ch3 control).

(refer register Address table in **Appendix A**)

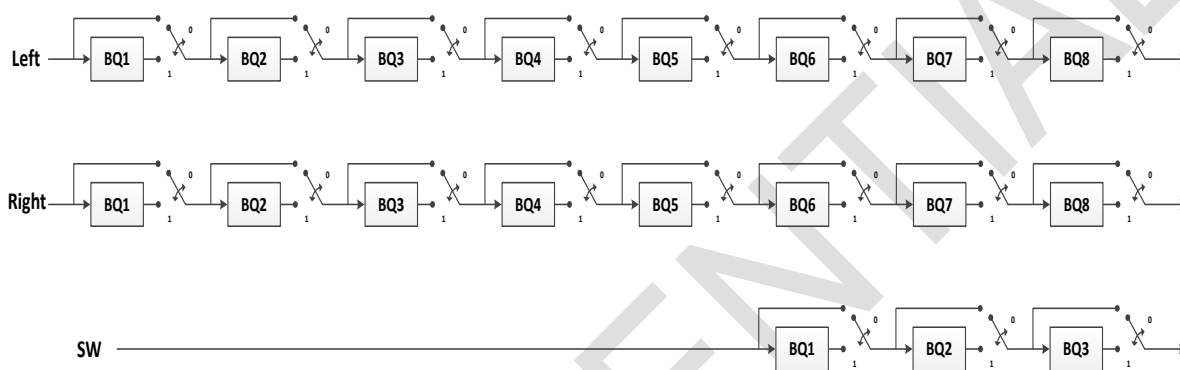


Figure 17. Post Bi-Quad Filter Structure

10. VOLUME & DYNAMIC RANGE CONTROL

Master and channel volumes of the NTP8808 are independently controlled and softly changed. The system register address 0x2E is the master volume control that affects 3 channels simultaneously and the address 0x2F, 0x30 and 0x31 correspond to the channel volume control register for channel 1, 2 and 3 respectively.

The possible Maximum Gain is +48.375dB with using master volume fine control, master volume and channel volume because the master volume applies the gain to an input signal independent from a channel volume. However, in such a case, a clipping might occur to prevent a signal overflow error if the magnitude of the input signal is large enough to exceed 0dB under the combined volume setting.

10.1. Master Volume Control

By setting volume control register (address 0x2E), master volume is controlled from negative infinity through 24dB with selectable step size as follows. For details on the master volume setting, see the register value table shown in **Appendix B**.

| Step | Range |
|--------|----------------|
| 0.5 dB | +24 ~ -100 dB |
| 10 dB | -100 ~ -150 dB |

Table 4. Level Dependent Master Volume Steps

10.2. Channel Volume Control

By setting volume control registers (address 0x2F~0x31), channel volumes are independently controlled from negative infinity through +24dB with two selectable step sizes as described below, and in the **Appendix B**, exact values for channel volume setting are described.

| Step | Range |
|--------|----------------|
| 0.5 dB | +24 ~ -100 dB |
| 10 dB | -100 ~ -150 dB |

Table 5. Level Dependent Channel Volume Steps

10.3. Master Volume Fine Control

Fine control for master volume is possible (+0.0625dB step up to maximum +0.4375dB boost). Refer the system register Address 0x2D in the **Appendix A**.

10.4. Mute and Soft Volume Change

The NTP8808 enters mute state by setting soft mute flag of register Address 0x26. Soft mute is implemented so that the volume gradually increases or decreases when mute is turned off or on respectively. Also the soft mute speed and soft volume change speed rates are programmable. Designers can minimize the pop noise by controlling the soft mute speed and volume change intervals. Refer SMH flag of register Address 0x26 and SVI flag of register Address 0x32.

10.5. Auto Mute

The NTP8808 can mute the sound automatically when the level of input audio signal is lower than the register-controlled threshold value. The mute can be done PWM switching with 50 % duty ratio in AD mode or with a high pulse duration of MLP width in D-BTL mode as shown in Figure 21. Auto mute is supported for internal channels 1~3 after 2x3 mixer block. Refer register Address 0x33 and 0x34.

10.6. Dynamic Range Control

Dynamic range control can be turned on or off with programmable compression threshold and attack/release rates. The threshold parameters of DRC can be controlled separately for channel 1/2 and channel 3. For detailed setting, please refer to the system register Addresses 0x1C~0x25 and refer to the coefficient mode register addresses in Table 6.

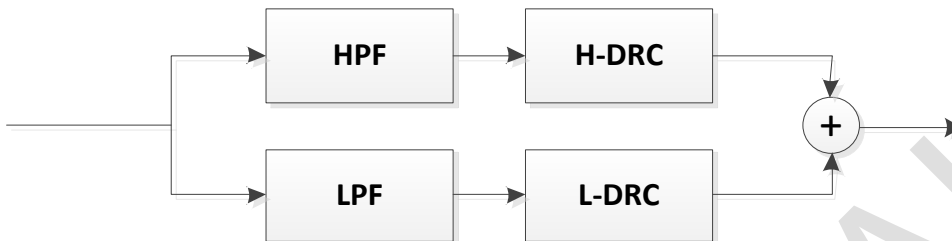


Figure 18. Block Diagram of Dynamic Range Control

| | | | | | | |
|---|-------------|-------------|-------------|-------------|-------------|-------------|
| 2B' DRC Coefficient Mode Register Address | 0x46 ~ 0x4A | 0x4B ~ 0x4F | 0x50 ~ 0x54 | 0x55 ~ 0x59 | 0x5A ~ 0x5E | 0x5F ~ 0x63 |
| When System Register Address 0x7E = 0x03 | BQ1_Low | BQ2_Low | BQ3_High | BQ4_High | Attack Low | Attack High |

| | | | | | | | |
|---------------------|----------------------|-----------------|------------------|--------------------|--------------------|---------------------|---------------------|
| 0x64 | 0x65 | 0x66 | 0x67 | 0x68 | 0x69 | 0x6A | 0x6B |
| Release Gain Low | Release Gain High | THD Gain Low | THD Gain High | PowerMeter Gain | Attack Gain Low | Attack Gain High | Attack Gain Post |

Table 6. DRC Coefficient Mode Register Map for Dynamic Range Control

11. OUTPUT INTERFACE

11.1. Output Configuration

The output mode of NTP8808 is 2.0 stereo reproduction mode and 2.1 reproduction mode. To produce proper output signal, register 0x35~0x37 should be set to appropriate values.

11.2. AM Interference Relief Mode

The NTP8808 has AM interference reduction mode. In this mode SNR performance of NTP8808 can be degrade down to 90 dB and the PWM switching frequency is spread from 384kHz through 768kHz.

11.3. PWM Output Mapper

Any internal channel that produces a PWM output can be assigned to any PWM output hardware port (or pin) by mapping output port register. This feature is very helpful for the hardware designer because it can relieve difficulties in the power stage signal routing and channel assignment if the output channel order is fixed. See the system register address 0x35~0x37 in the **Appendix A**.

11.4. Switching Output Mode

There are two selectable switching output modes in NTP8808. The difference between two output modes lies in the relationship of the relative signal pattern between PWM OUTxA and PWM OUTxB for a channel x. The first one is called as AD mode. This AD mode can be applied to both half bridge and full bridge output stage.

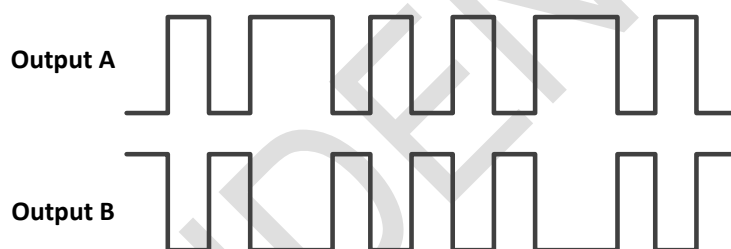


Figure 19. PWM Output Signals in AD Mode

AD asynchronous pair means the normal AD mode PWM output. In other words, A output and B output of each PWM output pair are mutually complementary. In the case of AD synchronous pair, A output and B output is perfectly identical, and its relation is not complementary. This is useful in some special case including single-ended power stage design.

The other one is called as NTX (Neo Trinity Amplification), which is D-BTL mode. This mode is applied only for BTL, and its operation is dynamically-biased BTL, compared to the normal BTL. An example of output signals in D-BTL mode is shown in **Figure 20**.

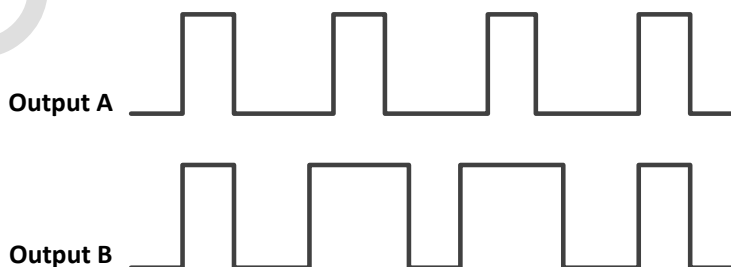


Figure 20. PWM Output Signals in D-BTL Mode

The MLP (Minimum Linear Pulse Length) is a key parameter in D-BTL mode. MLP defines the minimum pulse length that can guarantee a linear relationship between the input and output pulse length. Generally, the width of the output pulse is proportional to that of the input pulse. However, as the width of input pulse becomes narrower, such linear relation is not maintained due to the characteristic of a power device. The minimum MLP value is preferred as long as linear relationship between the input and the output pulse is satisfied. In addition, in terms of power consumption, a minimal MLP value is preferred.

This compensation is illustrated in **Figure 21**.

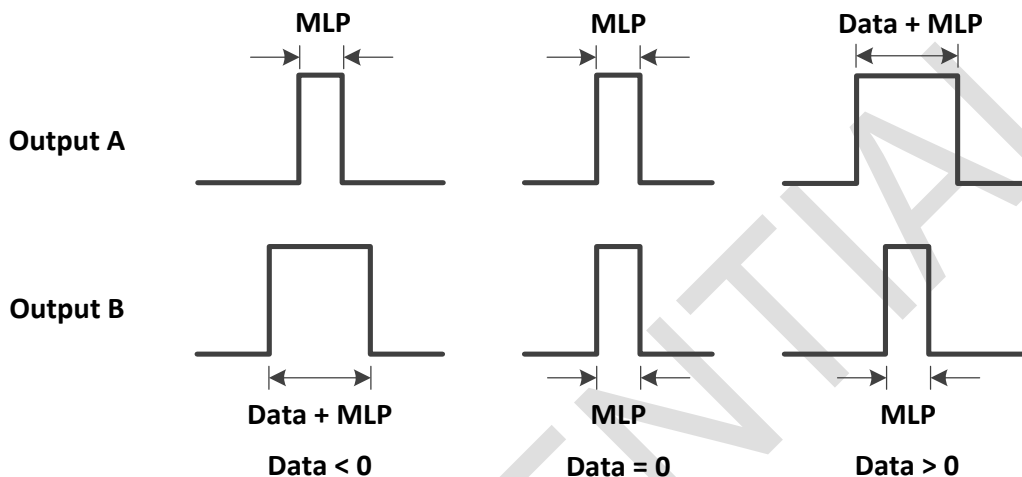


Figure 21. Compensation by MLP

11.5. Soft Start

The soft_start reduces pop noise by controlling rapidly increased energy of PWM in AD mode. To begin soft_start operation, PWM soft start enable register (0x52: PSE) should be set to high, and then PWM switching on/off register (0x27: POF) should be set to low. The duty ratio of PWM output increases from 127:1 (Low:High) to 50:50 (Low:High). Step repeat time register (0x52: SRT) means repeat number of PWM output. Soft_start operation with 17 repetitions is shown in the **Figure 22**.

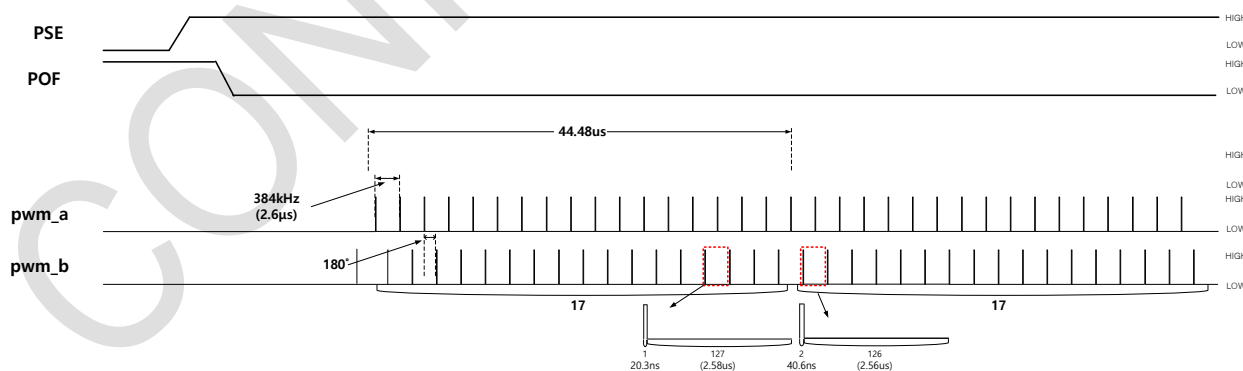
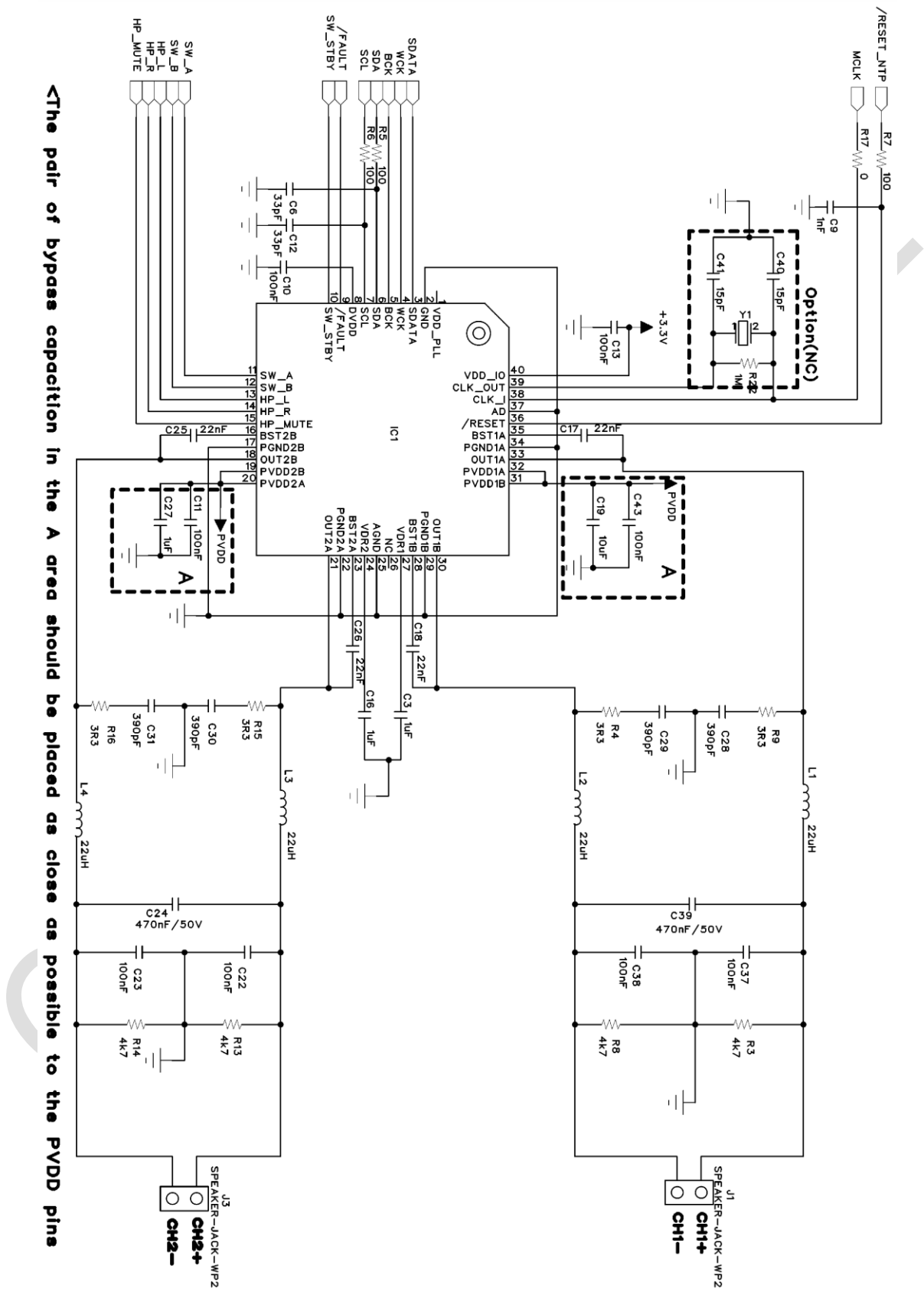


Figure 22. Soft Start Operation Timing

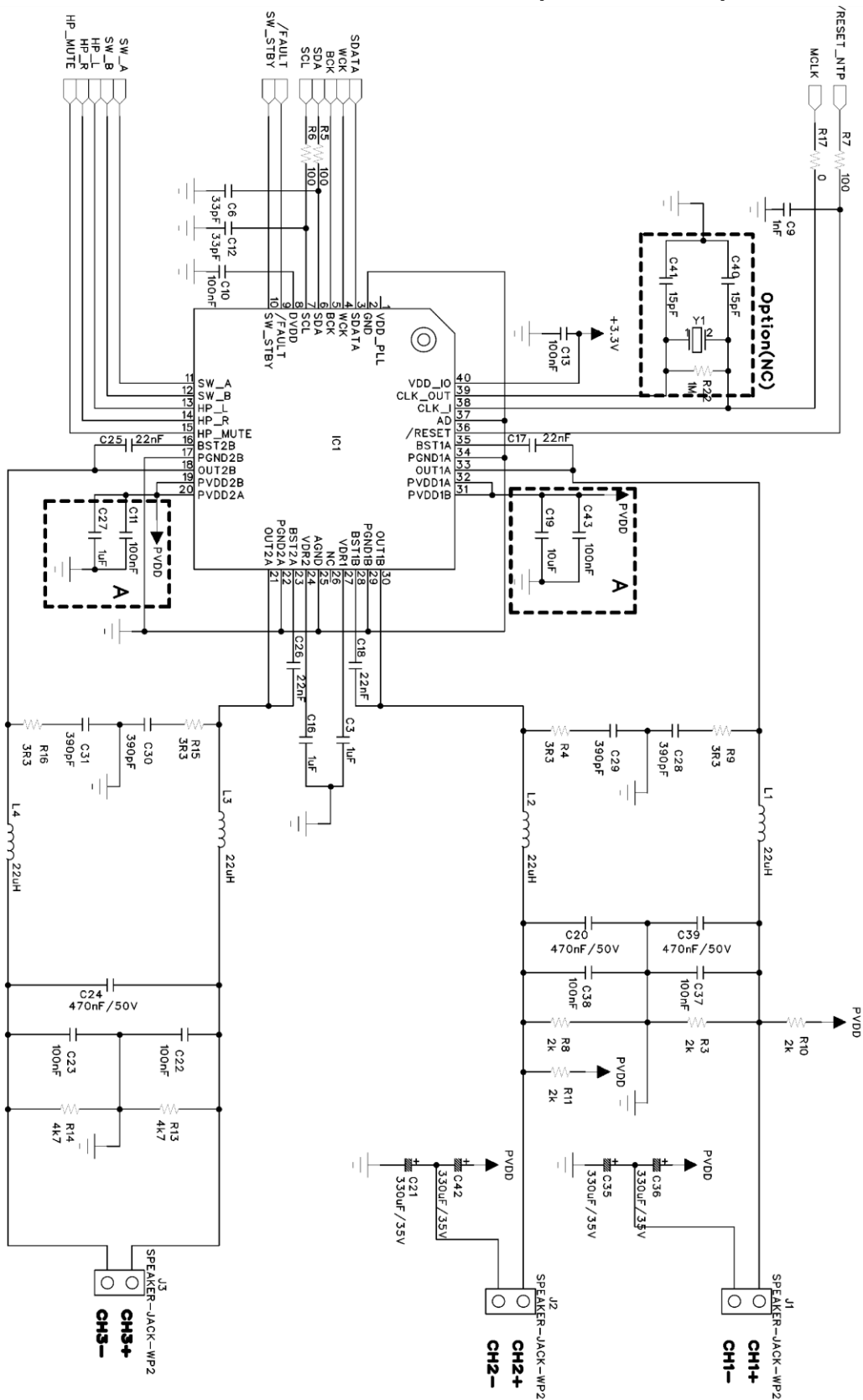
12.TYPICAL APPLICATION SCHEMATICS (2 Channel)



<The pair of bypass capciton in the A area should be placed as close as possible to the PVDD pins

13. TYPICAL APPLICATION SCHEMATICS (2.1 Channel)

<The pair of bypass capacitors in the A area should be placed as close as possible to the PVDD pins



14. APPENDIX

A. Configuration Register Summary

Addr 0x00: Audio Input Format

| | | | | | | | | |
|------|---|---|---|-----|---|---|-----|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | X | X | X | FSM | | | INS | |

| Name | Description | Value | Meaning | Ref. |
|------|--|--------------|-----------------------------------|------|
| INS | Input format | b'00 | I ² S, slave mode | |
| | | b'01 | I ² S, master mode | |
| | | b'10 | General serial audio, slave mode | |
| | | b'11 | General serial audio, master mode | |
| FSM | Sampling Frequency in Master mode I ² S | b'000 | 48 kHz | |
| | | b'001 | 8 kHz | |
| | | b'010 | 16 kHz | |
| | | b'011 | 32 kHz | |
| | | b'100 | 12 kHz | |
| | | b'101 | 24 kHz | |
| | | b'110 | 96 kHz | |
| | | b'111 | 192 kHz | |

Addr 0x01: General Serial Audio Format

| | | | | | | | | |
|------|---|---|------|---|----|---|-----|-----|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | X | X | BCKS | | BS | | MLF | LRJ |

| Name | Description | Value | Meaning | Ref. |
|------|-----------------------|-------------|---------------|------|
| LRJ | Serial data justify | b'0 | Left justify | |
| | | b'1 | Right justify | |
| MLF | Serial bit order | b'0 | MSB first | |
| | | b'1 | LSB first | |
| BS | Serial bit size | b'00 | 24 bit | |
| | | b'01 | 20 bit | |
| | | b'10 | 18 bit | |
| | | b'11 | 16 bit | |
| BCKS | Bit clock size select | b'00 | 64 BCK/WCK | |
| | | b'01 | 48 BCK/WCK | |
| | | b'10 | 32 BCK/WCK | |

Addr 0x02: Master Clock Frequency Control

| | | | | | | | | |
|------|---|---|---|---|---|---|-----|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | X | X | X | X | X | X | MCF | |

| Name | Description | Value | Meaning | Ref. |
|------|------------------------|-------------|------------|------|
| MCF | Master Clock Frequency | b'00 | 12.288 MHz | |
| | | b'01 | 24.576 MHz | |
| | | b'10 | 18.432 MHz | |

Addr 0x03~0x08: Mixer Gain

| | | | | | | | | |
|------|---|----|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | X | MG | | | | | | |

| Name | Description | Value | Meaning | Ref. |
|------|-------------|----------------|----------------------------------|------|
| MG | Mixer gain | h'00 ~ h'7F | Mixer gain (refer to gain table) | |

Reserved Addr 0x09~0x0B**Addr 0x0C : Front Bi-quad Filter Chain (FBQ) Configurations for Ch 1&2&3**

| | | | | | | | | |
|------|---|---|-------|-------|-------|-------|-------|-------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | X | X | FBQ32 | FBQ31 | FBQ22 | FBQ21 | FBQ12 | FBQ11 |

| Name | Description | Value | Meaning | Ref. |
|-------|----------------------------------|-------|---------|------|
| FBQ11 | 1 st FBQ flag for CH1 | b'0 | Bypass | |
| | | b'1 | Enable | |
| FBQ12 | 2nd FBQ flag for CH1 | b'0 | Bypass | |
| | | b'1 | Enable | |
| FBQ21 | 1 st FBQ flag for CH2 | b'0 | Bypass | |
| | | b'1 | Enable | |
| FBQ22 | 2nd FBQ flag for CH2 | b'0 | Bypass | |
| | | b'1 | Enable | |
| FBQ31 | 1 st FBQ flag for CH3 | b'0 | Bypass | |
| | | b'1 | Enable | |
| FBQ32 | 2nd FBQ flag for CH3 | b'0 | Bypass | |
| | | b'1 | Enable | |

Reserved Addr 0x0D~0x14**Addr 0x15: CH1&CH2 Prescaler Value Configuration**

| | | | | | | | | |
|------|----|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | PS | | | | | | | |

| Name | Description | Value | Meaning | Ref. |
|------|-------------|----------------|----------------------------|------|
| PS | Prescaler | h'00 ~ h'FF | 208 (0xD0)default | |

Addr 0x16: CH3 Prescaler Value Configuration

| | | | | | | | | |
|------|----|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | PS | | | | | | | |

| Name | Description | Value | Meaning | Ref. |
|------|-------------|----------------|----------------------------|------|
| PS | Prescaler | h'00 ~ h'FF | 208 (0xD0)default | |

Addr 0x17~0x18: Post Biquad Filter (PBQ) Configuration0 for Ch 1 and Ch2, respectively

| | | | | | | | | |
|------|---|---|---|-----|-----|-----|-----|-----|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | X | X | X | BQ5 | BQ4 | BQ3 | BQ2 | BQ1 |

| Name | Description | Value | Meaning | Ref. |
|------|-------------------------------------|------------|-------------------------------|------|
| BQ1 | On/off Bi-Quad 1 of ch. n (n= 1,2) | b'0 | Bypass Bi-Quad 1 of channel n | |
| | | b'1 | Enable Bi-Quad 1 of channel n | |
| BQ2 | On/off Bi-Quad 2 of ch. n (n= 1,2) | b'0 | Bypass Bi-Quad 2 of channel n | |
| | | b'1 | Enable Bi-Quad 2 of channel n | |
| BQ3 | On/off Bi-Quad 3 of ch. n (n = 1,2) | b'0 | Bypass Bi-Quad 3 of channel n | |
| | | b'1 | Enable Bi-Quad 3 of channel n | |
| BQ4 | On/off Bi-Quad 4 of ch. n (n = 1,2) | b'0 | Bypass Bi-Quad 4 of channel n | |
| | | b'1 | Enable Bi-Quad 4 of channel n | |
| BQ5 | On/off Bi-Quad 5 of ch. n (n = 1,2) | b'0 | Bypass Bi-Quad 5 of channel n | |
| | | b'1 | Enable Bi-Quad 5 of channel n | |

Addr 0x19~0x1A : Post Biquad Filter (PBQ) Configuration1 for Ch 1 and Ch 2, respectively

| | | | | | | | | |
|------|---|---|-----|---|-----|---|-----|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | X | X | BQ8 | | BQ7 | | BQ6 | |

| Name | Description | Value | Meaning | Ref. |
|------|-------------------------------------|-------------|-------------------------------|------|
| BQ6 | On/off Bi-Quad 6 of ch. n (n = 1,2) | b'00 | Bypass Bi-Quad 6 of channel n | |
| | | b'01 | Enable Bi-Quad 6 of channel n | |
| BQ7 | On/off Bi-Quad 7 of ch. n (n = 1,2) | b'00 | Bypass Bi-Quad 7 of channel n | |
| | | b'01 | Enable Bi-Quad 7 of channel n | |
| BQ8 | On/off Bi-Quad 8 of ch. n (n = 1,2) | b'00 | Bypass Bi-Quad 8 of channel n | |
| | | b'01 | Enable Bi-Quad 8 of channel n | |

Addr 0x1B : Post Biquad Filter (PBQ) Configuration for Ch 3

| | | | | | | | | |
|------|---|---|-----|---|-----|---|-----|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | X | X | BQ3 | | BQ2 | | BQ1 | |

| Name | Description | Value | Meaning | Ref. |
|------|--------------------------|-------------|-------------------------------|------|
| BQ1 | On/off Bi-Quad 1 of ch 3 | b'00 | Bypass Bi-Quad 1 of channel n | |
| | | b'01 | Enable Bi-Quad 1 of channel n | |
| BQ2 | On/off Bi-Quad 2 of ch 3 | b'00 | Bypass Bi-Quad 2 of channel n | |
| | | b'01 | Enable Bi-Quad 2 of channel n | |
| BQ3 | On/off Bi-Quad 3 of ch 3 | b'00 | Bypass Bi-Quad 3 of channel n | |
| | | b'01 | Enable Bi-Quad 3 of channel n | |

Addr 0x1C: DRC Control 0

| | | | | | | | | |
|------|-------|-------|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | CPR_L | CTS_L | | | | | | |

| Name | Description | Value | Meaning | Ref. |
|-------|----------------------------|-----------------------------------|--|------|
| CTS_L | DRC threshold for low band | b'000 0000 ~ b'111 1111 | -57 ~ 12dB unsigned 7-bit DRC threshold for 1 band mode. In 2 band mode, it will control the threshold of low band. Refer to DRC threshold value table for threshold values. | |
| CPR_L | DRC enable for low band | b'0 | Dynamic Range Compression off | |
| | | b'1 | Dynamic Range Compression on | |

Addr 0x1D : DRC Control 1

| | | | | | | | | |
|------|---|-------|---|---|---|-------|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | X | C1C_L | | | X | A1C_L | | |

| Name | Description | Value | Meaning | Ref. |
|-------|-----------------------------|-------------------------|---|------|
| A1C_L | DRC attack time (low band) | b'000 ~ b'111 | Attack time control for 1 band mode. In 2 band mode, it will control the attack time of low band. (See attack time table below.) (default = b'001) | |
| C1C_L | DRC release time (low band) | b'000 ~ b'111 | Release time control for 1 band mode. In 2 band mode, it will control the release time of low band. (See release time table below.) | |

| Value of Register | Attack time 6dB, fs = 96,000 |
|-------------------|---------------------------------|
| 011 | 30 msec |
| 010 | 15 msec |
| 001 | 8 msec |
| 000 | 4 msec |
| 111 | 2 msec |
| 110 | 1 msec |
| 101 | 0.5 msec |
| 100 | 0.25 msec |

Table 7. DRC Attack Time Table

| Value of Register | Release time 6dB, fs = 96,000 |
|-------------------|----------------------------------|
| 011 | 5.0 sec |
| 010 | 2.0 sec |
| 001 | 1.0 sec |
| 000 | 0.5 sec |
| 111 | 0.2 sec |
| 110 | 0.1 sec |
| 101 | 0.05sec |
| 100 | 0.025sec |

Table 8. DRC Release Time Table

Addr 0x1E : DRC Control 2

| | | | | | | | | |
|------|-------|-------|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | CPR_H | CTS_H | | | | | | |

| Name | Description | Value | Meaning | Ref. |
|-------|-----------------------------|-----------------------------------|--|------|
| CTS_H | DRC threshold for high band | b'000 0000 ~ b'111 1111 | -57 ~ 12dB unsigned 7-bit DRC threshold for high band. It has effect only in 2 band mode. Refer to DRC threshold value table for threshold values. | |
| CPR_H | DRC enable for high band | b'0 | Dynamic Range Compression off | |
| | | b'1 | Dynamic Range Compression on | |

Addr 0x1F : DRC Control3

| | | | | | | | | |
|------|---|-------|---|---|---|-------|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | X | C1C_H | | | X | A1C_H | | |

| Name | Description | Value | Meaning | Ref. |
|-------|------------------------------|-------------------------|--|------|
| A1C_H | DRC attack time (high band) | b'000 ~ b'111 | Attack time control for high band mode. It has effect only in 2 band mode. (default = b'001) (See attack time table in Addr 0x1D.) | |
| C1C_H | DRC release time (high band) | b'000 ~ b'111 | Release time control for high band mode. It has effect only in 2 band mode. (See release time table in Addr 0x1D.) | |

Addr 0x20 : DRC Control 4

| | | | | | | | | |
|------|--------|--------|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | CPR_SW | CTS_SW | | | | | | |

| Name | Description | Value | Meaning | Ref. |
|--------|--------------------------|----------------------------------|---|------|
| CTS_SW | DRC threshold | b'000 0000 ~b'111 1111 | Sub-woofer uses 1-band DRC -57 ~ 12dB unsigned 7-bit DRC threshold When ch1 and ch2 is working in 2band mode, this will be effective. | |
| CPR_SW | DRC enable for high band | b'0 | Dynamic Range Compression off | |
| | | b'1 | Dynamic Range Compression on | |

Addr 0x21: DRC Control 5

| | | | | | | | | |
|------|---|--------|---|---|---|--------|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | X | C1C_SW | | | X | A1C_SW | | |

| Name | Description | Value | Meaning | Ref. |
|--------|------------------|-------------------------|--|------|
| A1C_SW | DRC attack time | b'000 ~ b'111 | Attack time control for sub-woofer. (default = b'001) When ch1 and ch2 is in 2band mode, it will be effective. (See attack time table in Addr 0x1D.) | |
| C1C_SW | DRC release time | b'000 ~ b'111 | Release time control for sub-woofer. When ch1 and ch2 is in 2band mode, it will be effective. (See release time table in Addr 0x1D.) | |

Addr 0x22 : DRC Control 6

| | | | | | | | | |
|------|-------|-------|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | CPR_P | CTS_P | | | | | | |

| Name | Description | Value | Meaning | Ref. |
|-------|------------------------------|-----------------------------------|--|------|
| CTS_P | DRC threshold for post- band | b'000 0000 ~ b'111 1111 | -57 ~ 12dB unsigned 7-bit DRC threshold Refer to DRC threshold value table. | |
| CPR_P | DRC enable for post-band | b'0 | Dynamic Range Compression off | |
| | | b'1 | Dynamic Range Compression on | |

Addr 0x23: DRC Control 7

| | | | | | | | | |
|------|---|-------|---|---|---|-------|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | X | C1C_P | | | X | A1C_P | | |

| Name | Description | Value | Meaning | Ref. |
|-------|-----------------------------|------------------|---|------|
| A1C_P | DRC attack time (post-DRC) | b'000 ~ b'111 | Attack time (default = b'001) | |
| C1C_P | DRC release time (post-DRC) | b'000 ~ b'111 | Release time (default = b'100) | |

Addr 0x24 : DRC Control 8

| | | | | | | | | |
|------|---|---|---|-----|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | X | X | X | DLL | | | | |

| Name | Description | Value | Meaning | Ref. |
|------|-------------------|-----------------------|----------------------------------|------|
| DLL | Delay line length | h'00 ~ h'14 | Delay line length. 0~20(decimal) | |

Addr 0x25 : DRC Control 9

| | | | | | | | | |
|------|-----|------|------|-----|-----|-----|-----|-----|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | CCO | DTS1 | DTS2 | 2BM | ASB | RSB | TSB | CAS |

| Name | Description | Value | Meaning | Ref. |
|------|----------------------------------|-------|---|------|
| CAS | Coupled Allpass Structure enable | b'0 | Enable coupled allpass structure | |
| | | b'1 | Disable coupled allpass structure | |
| TSB | Threshold parameter select bit | b'0 | Uses Threshold parameters in Table | |
| | | b'1 | Uses Threshold parameters from external loading | |
| RSB | Release parameter select bit | b'0 | Uses Release parameters in Table | |
| | | b'1 | Uses Release parameters from external loading | |
| ASB | Attack parameter select bit | b'0 | Uses Attack parameters in Table | |
| | | b'1 | Uses Attack parameters from external loading | |
| 2BM | 2band mode enable | b'0 | 1 band DRC | |
| | | b'1 | 2 band DRC | |
| DTS2 | P-DRC type select | b'0 | P-DRC new mode | |
| | | b'1 | P-DRC old mode | |
| DTS1 | LH-DRC type select | b'0 | LH-DRC new mode | |
| | | b'1 | LH-DRC old mode | |
| CCO | Clip control option | b'0 | Clip on | |
| | | b'1 | Clip off | |

※ case. 1band DRC : CAS must be enabled.

Addr 0x26 : Soft Mute Control 0

| | | | | | | | | |
|------|-----|---|---|---|---|-----|-----|-----|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | SMH | X | X | X | X | SM3 | SM2 | SM1 |

| Name | Description | Value | Meaning | Ref. |
|------|----------------|-------|----------------------------|------|
| SMn | Softmute | b'0 | increase for channel n | |
| | | b'1 | decrease for channel n | |
| SMH | Softmute speed | b'0 | 42/46 msec(at 96/88.2kHz)) | |
| | | b'1 | Hard change | |

Addr 0x27 : PWM Switching On/Off Control

| | | | | | | | | |
|------|---|---|---|---|---|------|------|------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | X | X | X | X | X | POF3 | POF2 | POF1 |

| Name | Description | Value | Meaning | Ref. |
|------|---------------------------------|-------|-----------------------------|------|
| POFn | Switching output On/off control | b'0 | Channel n PWM switching on | |
| | | b'1 | Channel n PWM switching off | |

Addr 0x28 : PWM_MASK Control 0

| | | | | | | | | |
|------|---|---|---|---|-----|-------|------|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | X | X | X | X | SRD | FPMLD | PWMM | |

| Name | Description | Value | Meaning | Ref. |
|-------|-------------------------------------|-------------|--|------|
| PWMM | PWM MASK register | b'10 | PWM MASK output is low. (reset default) | |
| | | otherwise | PWM MASK output is high. | |
| FPMLD | Permanent PWM_MASK Low disable flag | b'0 | No effect | |
| | | b'1 | Reset the auto_PWM_MASK_restore_counter to 0 | |
| SRD | FAULT disable | b'0 | FAULT is effect for PROTECT | |
| | | b'1 | FAULT is ineffective for PROTECT | |

Addr 0x29: PWM_MASK Control 1

| | | | | | | | | |
|------|---|---|---|---|---|---|-----|-----|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | X | X | X | X | X | X | APM | POF |

| Name | Description | Value | Meaning | Ref. |
|------|---------------|------------|--|------|
| POF | PWM off flag | b'0 | Even if Auto PWM_MASK condition is met, the PWM output of all channel is not affected. | |
| | | b'1 | When Auto PWM_MASK condition is met, the PWM output of all channel goes to the defined state which is set by the PWM off state control register (Addr 0x2A). | |
| APM | PWM_MASK flag | b'0 | Even if Auto PWM_MASK condition is met, the PWM_MASK output of all channel is not affected. | |
| | | b'1 | When Auto PWM_MASK condition is met, the PWM_MASK output goes to Low state. | |

Addr 0x2A : PWM_MASK Control 2

| | | | | | | | | |
|------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | VMSK3 | VMSK2 | VMSK1 | VMSK0 | PMSK3 | PMSK2 | PMSK1 | PMSK0 |

| Name | Description | Value | Meaning | Ref. |
|------|--------------------------------|------------|---|------|
| PMSK | Masking bit of PWM off control | b'0 | Mask bit indicating the validity of n-th bit of Addr 0x5E system register: If the n-th bit of this register is zero, the n-th bit of Addr 0x5E system register is invalid. The n-th bit of Addr 0x5E is valid only when the n-th mask bit is one. | |
| | | b'1 | | |
| VMSK | Masking bit of PWM_MASK signal | b'0 | | |
| | | b'1 | | |

Addr 0x2B : PWM_MASK Control 3

| | | | | | | | | |
|------|-----|---|-------|---|---|-----|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | IRC | | AVRCT | | | PHT | | |

| Name | Description | Value | Meaning | Ref. |
|-------|--|--------------|----------------------------|------|
| PHT | PWM_MASK Low Hold Time | b'000 | 0.5 msec Hold Time | |
| | | b'001 | 1 msec Hold Time | |
| | | b'010 | 2 msec Hold Time | |
| | | b'011 | 4 msec Hold Time (Default) | |
| | | b'100 | 8 msec Hold Time | |
| | | b'101 | 16msec Hold Time | |
| AVRCT | Auto PWM_MASK Restore Counter Threshold | b'000 | 2 | |
| | | b'001 | 5 (Default) | |
| | | b'010 | 10 | |
| | | b'011 | 15 | |
| | | b'100 | 20 | |
| | | b'101 | 25 | |
| | | b'110 | 30 | |
| IRC | Auto PWM_MASK Restore Interval Ratio Control | b'00 | 2 (Default) | |
| | | b'01 | 4 | |

Addr 0x2C: PWM_MASK Control 4

| | | | | | | | | |
|------|-----|-----|---|---|---|-----|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | SHE | POE | X | X | X | HT2 | | |

| Name | Description | Value | Meaning | Ref. |
|------|--|--------------|------------------------------|------|
| HT2 | Hold Time 2 apply start point (restore counter) | b'000 | 100 msec Hold Time | |
| | | b'001 | 200 msec Hold Time | |
| | | b'010 | 400 msec Hold Time | |
| | | b'011 | 600 msec Hold Time (Default) | |
| | | b'100 | 800 msec Hold Time | |
| | | b'101 | 1 sec Hold Time | |
| | | b'110 | 2 sec Hold Time | |
| POE | PWM off when Fault detected and PWM on when PWM_MASK Recover | b'0 | Disable | |
| | | b'1 | Enable (Default) | |
| SHE | Second Hold time Enable | b'0 | Disable (Default) | |
| | | b'1 | Enable | |

Addr 0x2D: Master Volume Fine Control

| | | | | | | | | |
|------|---|---|---|---|---|------|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | X | X | X | X | X | MVFC | | |

| Name | Description | Value | Meaning | Ref. |
|------|----------------------------|---------------------|-----------------------------------|------|
| MVFC | Master volume fine control | h'0 ~ h'7 | 0 dB ~ 0.5 dB with 0.0625 dB step | |

Addr 0x2E~0x31: Master Volume, and Ch1/2/3 volume, respectively

| | | | | | | | | |
|------|-----|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | VOL | | | | | | | |

| Name | Description | Value | Meaning | Ref. |
|------|----------------|----------------|--|------|
| VOL | Volume control | h'00 ~ h'FF | See volume control register tables. Reset default is 0 (0x00) (= $-\infty$ dB)for Master and 207 (0xCF) for Channel | |

Addr 0x32: Soft Volume Control

| | | | | | | | | |
|------|---|---|---|---|---|---|-----|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | X | X | X | X | X | X | SVI | |

| Name | Description | Value | Meaning | Ref. |
|------|--------------------|-------|----------------------------|------|
| SVI | Soft volume change | b'00 | Medium speed | |
| | | b'01 | High speed | |
| | | b'10 | Low speed | |
| | | b'11 | soft volume change disable | |

Addr 0x33: Auto-Mute Control for CH1 & CH2

| | | | | | | | | |
|------|---|------|----|---|----|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | X | EAMC | II | | AT | | | |

| Name | Description | Value | Meaning | Ref. |
|------|-------------------------------|--------------------|-----------------------------------|------|
| AT | Auto-mute detection threshold | b'0000 ~ b'1111 | Unsigned integer between 0 and 15 | |
| II | Auto-mute response time | b'00 | 5 msec | |
| | | b'01 | 50 msec | |
| | | b'10 | 500 msec | |
| | | b'11 | 2 sec | |
| EAMC | Effect of Auto-mute condition | b'0 | Auto mute disable(No-Effect) | |
| | | b'1 | Continue switching if auto-mute | |

Addr 0x34: Auto-Mute Control for CH3

| | | | | | | | | |
|------|---|------|----|---|----|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | X | EAMC | II | | AT | | | |

| Name | Description | Value | Meaning | Ref. |
|------|-------------------------------|--------------------|-----------------------------------|------|
| AT | Auto-mute detection threshold | b'0000 ~ b'1111 | Unsigned integer between 0 and 15 | |
| II | Auto-mute response time | b'00 | 5 msec | |
| | | b'01 | 50 msec | |
| | | b'10 | 500 msec | |
| | | b'11 | 2 sec | |
| EAMC | Effect of Auto-mute condition | b'0 | Auto mute disable(No-Effect) | |
| | | b'1 | Continue switching if auto-mute | |

Reserved Addr 0x35~0x37

Addr 0x38: Miscellaneous PWM Control

| | | | | | | | | |
|------|---|---|---|-----|-----|-----|----|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | X | X | X | POL | BHL | AHL | MD | |

| Name | Description | Value | Meaning | Ref. |
|------|-----------------------------------|-------------|---------------------------------------|------|
| MD | PWM output mode | b'00 | AD mode with asynchronous signal pair | |
| | | b'01 | AD mode with synchronous signal pair | |
| | | b'10 | PWM D-BTL MODE (see 0x4E) | |
| | | b'11 | AM Interference mode | |
| AHL | A-out state When switching off | b'0 | Low | |
| | | b'1 | High | |
| BHL | B-out state when switching off | b'0 | Low | |
| | | b'1 | High | |
| POL | Ch3 polarity Control | b'0 | Normal | |
| | | b'1 | Inverse | |

Addr 0x39: I²C Glitch filter

| | | | | | | | | |
|------|-----|-----|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | GFO | DUR | | | | | | |

| Name | Description | Value | Meaning | Ref. |
|------|---------------------------------|----------------------------|---|------|
| DUR | glitch width | b'000 0000 ~ b'111 1111 | minimum pulse width = DUR + 20 ns reset default = 15 * 10 ns (DUR default = b'0001111) | |
| GFO | Glitch filter enable/disable | b'0 | Glitch filter on | |
| | | b'1 | Bypass | |

Addr 0x3A : Headphone Mute Control

| | | | | | | | | |
|------|---|---|---|---|---|---|---|---------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | X | X | X | X | X | X | X | HP_MUTE |

| Name | Description | Value | Meaning | Ref. |
|---------|--|------------|---|------|
| HP_MUTE | Use this register to mute external headphone | b'0 | Default. External headphone is muted by active low signal | |
| | | b'1 | External headphone is muted by active high signal. | |

Reserved Addr 0x3B~0x49**Addr 0x4A : SE Soft Start Control 0**

| | | | | | | | | |
|------|---|---|---|---|---|---|---|-----|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | X | X | X | X | X | X | X | SSE |

| Name | Description | Value | Meaning | Ref. |
|------|-------------|------------|---|------|
| SSE | SE_STE | b'0 | SE Soft Start Disable (SE Normal Start) | |
| | | b'1 | SE Soft Start Enable | |

Addr 0x4B : SE Soft Start Control 1

| | | | | | | | | |
|------|---|-----|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | X | SSC | | | | | | |

| Name | Description | Value | Meaning | Ref. |
|------|----------------|----------------|---|------|
| SSC | SE_CHARGE_TIME | h'00 ~ h'7F | PWM output delay time from point of PWM STBY signal to high. The unit of 1bit is 10ns. (default : 0x22) | |

Addr 0x4C : SE Soft Start Control 2

| | | | | | | | | |
|------|-----|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | SSR | | | | | | | |

| Name | Description | Value | Meaning | Ref. |
|------|-------------|----------------|--|------|
| SSR | SE_REAPEAT | h'01 ~ h'FF | The repeat time of se soft start (default: 1 – means repeat 1 times) | |

Addr 0x4D : SE Soft Start Control 3

| | | | | | | | | |
|------|-----|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | SPD | | | | | | | |

| Name | Description | Value | Meaning | Ref. |
|------|-------------|----------------|--|------|
| SPD | SE_PERIOD | h'01 ~ h'7E | Half period of PWM output start point. The unit of 1bit is 10ns. (default : 0x01 – means half period 20ns) | |

Addr 0x4E : PWM D-BTL MODE Control 0

| | | | | | | | | |
|------|---|-----|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | X | MLP | | | | | | |

| Name | Description | Value | Meaning | Ref. |
|------|-----------------------------|-------|--|------|
| MLP | Minimum Linear pulse length | h'08 | Range : Minimum Pulse Width ~ 640ns, 20ns step.(refer Addr 0x45 for Minimum Pulse Width) | |

Reserved Addr 0x4F**Addr 0x50 : PWM D-BTL Mode Control 1**

| | | | | | | | | | |
|------|---|---|---|---|---|---|---|-----|--|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Name | X | | | | | | | NSS | |

| Name | Description | Value | Meaning | Ref. |
|------|-------------|-------|---------------------------|------|
| NSS | NS Select | b'00 | 7bits NS (AD mode) | |
| | | b'01 | Reserved | |
| | | b'10 | 8bits NS | |
| | | b'11 | New 8bits NS (D-BTL mode) | |

Reserved Addr 0x51**Addr 0x52 : PWM Soft Start**

| | | | | | | | | |
|------|-----|-----|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | PSE | SRT | | | | | | |

| Name | Description | Value | Meaning | Ref. |
|------|------------------------------|----------------------------|---|--|
| SRT | Step Repeat Time | b'000 0000 ~ b'111 1111 | The repeat time of each step (default : b'0010000 – means repeat 17 times) | |
| PSE | BTL PWM soft start Enable | b'0 | Disable | In Single Ended Mode, should be disabled |
| | | b'1 | Enable (Default) | |

Addr 0x53: Power Meter Control

| | | | | | | | | |
|------|---|---|---|-------|---|---|------|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | X | X | X | PDPOS | X | X | PDCH | |

| Name | Description | Value | Meaning | Ref. |
|-------|--------------------------------|-------|------------------------|------|
| PDCH | Power meter Detect Channel | b'00 | L+R (default) | |
| | | b'01 | L channel | |
| | | b'10 | R channel | |
| | | b'11 | reserved | |
| PDPOS | Power meter Detect Position | b'0 | After volume (default) | |
| | | b'1 | Before volume | |

Addr 0x54: Power Meter (read-only)

| | | | | | | | | |
|------|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Addr 0x55: Modulation Index & NS-Type Control

| | | | | | | | | |
|------|---|----|---|----|-----|---|------|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | X | M0 | | NT | MD3 | | MD12 | |

| Name | Description | Value | Meaning | Ref. |
|------|---|-------|--|------|
| MD12 | Modulation index control by Minimum pulse width for Ch 1&2 | b'00 | Minimum pulse width = 80ns | |
| | | b'01 | Minimum pulse width = 60ns | |
| | | b'10 | Minimum pulse width = 40ns | |
| | | b'11 | Minimum pulse width = 20ns | |
| MD3 | Modulation index control by Minimum pulse width for Ch 3 | b'00 | Minimum pulse width = 80ns | |
| | | b'01 | Minimum pulse width = 60ns | |
| | | b'10 | Minimum pulse width = 40ns | |
| | | b'11 | Minimum pulse width = 20ns | |
| NT | Noise shaping Type for Ch 1&2 | b'0 | Type 1 (fourth order) | |
| | | b'1 | Type 2 (fifth order) | |
| M0 | Dither Position Selector | b'00 | No left shift on dither value = Dither off | |
| | | b'01 | 1bit left shift on dither value | |
| | | b'10 | 2bit left shift on dither value | |
| | | b'11 | 3bit left shift on dither value | |

Addr 0x56: ASRC Control 0

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|-------|---|-------|-------|---|--------|
| Name | X | X | DCESW | X | FSFHM | FSFSM | X | BYPASS |

| Name | Description | Value | Meaning | Ref. |
|--------|---|-------|--|------|
| BYPASS | Bypass | b'0 | Normal operation | |
| | | b'1 | Bypass | |
| FSFSM | frequency stable effect on soft mute flag | b'0 | no effect on soft mute flag | |
| | | b'1 | soft mute flag = 1 when unstable state | |
| FSFHM | frequency stable effect on hard mute flag | b'0 | no effect on hard mute flag | |
| | | b'1 | hard mute flag = 1 when unstable state | |
| DCESW | DC Check Enable of SRC WCK | b'0 | DC Check Disable in SRC WCK | |
| | | b'1 | DC Check Enable in SRC WCK | |

Reserved Addr 0x57~0x5D**Addr 0x5E: System Error Status (read-only)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----|---|---|---|-----|------|------|-----|
| Name | FSI | | | | MPW | LSRC | ULCK | PPM |

| Name | Description | Value | Meaning | Ref. |
|--------|------------------------------------|--------|---|------|
| PPM | Permanent PWM_MASK Indication flag | b'0 | | |
| | | b'1 | Indicated that PWM_MASK is in Permanent LOW state | |
| ULCK | Sampled PLL Unlock error | b'0 | PLL is locked state. | |
| | | b'1 | PLL is unlocked state. | |
| LSRC | SRC lock status | b'0 | SRC is unlocked state. | |
| | | b'1 | SRC is locked state | |
| MPW | MCK/WCK Ratio error | b'0 | Ratio is incorrect. | |
| | | b'1 | Ratio is correct. | |
| FSI | Sampling Frequency Information | b'0000 | 8 kHz | |
| | | b'0001 | 11.025 KHz | |
| | | b'0010 | 12 kHz | |
| | | b'0011 | 16 kHz | |
| | | b'0100 | 22.025kHz | |
| | | b'0101 | 24 kHz | |
| | | b'0110 | 32 kHz | |
| | | b'0111 | 44.1 kHz | |
| | | b'1000 | 48 kHz | |
| | | b'1001 | 88.2 kHz | |
| | | b'1010 | 96 kHz | |
| b'1011 | 192 kHz | | | |

Addr 0x5F: Monitor

| | | | | | | | | |
|------|-----------|---|---|---|-----------|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | Monitor 1 | | | | Monitor 0 | | | |

| Name | Description | Value | Meaning | Ref. |
|-----------|--|---------------|----------------------------------|--|
| Monitor 0 | This output doesn't come through Power Device. | b'0000 | Soft_reset => Monitor 0 pin | In default, monitor 0/1 pin can be connected to woofer |
| | | b'0001 | Pwm1a=> Monitor 0 pin | |
| | | b'0010 | Pwm1b => Monitor 0 pin | |
| | | b'0011 | pwm2a => Monitor 0 pin | |
| | | b'0100 | Pwm2b => Monitor 0 pin | |
| | | b'0101 | Pwm3a => Monitor 0 pin | |
| | | b'0110 | Pwm3b => Monitor 0 pin | |
| | | b'0111 | Pwm_mask => Monitor 0 pin | |
| Monitor 1 | This output doesn't come through Power Device. | b'0000 | Soft_reset => Monitor 1 pin | |
| | | b'0001 | Pwm1a=> Monitor 1 pin | |
| | | b'0010 | Pwm1b => Monitor 1 pin | |
| | | b'0011 | pwm2a => Monitor 1 pin | |
| | | b'0100 | Pwm2b => Monitor 1 pin | |
| | | b'0101 | Pwm3a => Monitor 1 pin | |
| | | b'0110 | Pwm3b => Monitor 1 pin | |
| | | b'0111 | Pwm_mask => Monitor 1 pin | |
| | | b'1000 | SDATA_OUT => Monitor 0 pin | |
| | | b'1000 | SDATA_OUT => Monitor 1 pin | |

Addr 0x61: I2S Glitch Filter

| | | | | | | | | |
|------|-----|-----|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | GFE | WTH | | | | | | |

| Name | Description | Value | Meaning | Ref. |
|------|------------------------------|-----------------------------|--|------|
| WTH | glitch width | b'0000000 ~ b'1111111 | minimum pulse width = DUR + 20 ns reset default = 1 * 10 ns (DUR default = b'0000001) | |
| GFE | Glitch filter enable/disable | b'0 | Glitch filter on | |
| | | b'1 | Bypass | |

Addr 0x62: Driver Control

| | | | | | | | | |
|------|---|---|---|----|----|---|-----|------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | X | X | X | SB | PM | | KMS | SHDN |

| Name | Description | Value | Meaning | Ref. |
|------|----------------------------|-------------|--|------|
| SHDN | Shutdown | b'0 | SHDN pin go to high | |
| | | b'1 | SHDN pin go to low | |
| KMS | STBY signal output mode | b'0 | STBY : SB & PWM_MASK | |
| | | b'1 | STBY : SB | |
| PM | PWM Mode | b'00 | Normal Operation | |
| | | b'01 | 1 chip 2.1 channel mode (Single Ended Mode) cf) Should be disable 0x52 PSE | |
| | | b'10 | 1 chip 2.0 channel mode or 2.1 channel with external power stage (BTL Mode) cf) Should be disable 0x4A SSE | |
| SB | Stand-by in 2 channel mode | b'0 | Power Device: Stand-by operation | |
| | | b'1 | Power Device: Normal operation | |

Reserved Addr 0x63~0x65**Addr 0x66: Power-Die Status (Read-Only)**

| | | | | | | | | |
|------|---|---|---|---|---|---|-----|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | X | X | X | X | X | X | PDS | |

| Name | Description | Value | Meaning | Ref. |
|------|------------------|-------------|------------------------------|------|
| PDS | Power-Die Status | b'00 | Normal State | |
| | | b'01 | Temperature Protection Error | |
| | | b'10 | Voltage Protection Error | |
| | | b'11 | Current Protection Error | |

Reserved Addr 0x67~0x7D**Addr 0x7E: Bi-Quad Filter Coefficient Page**

| | | | | | | | | |
|------|---|---|---|---|-----|-----|-----|-----|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | X | X | X | X | PEQ | CH3 | CH2 | CH1 |

| Name | Description | Value | Meaning | Ref. |
|------|--------------------------|------------|-----------------------------------|------|
| CH1 | Coefficient write enable | b'0 | Disable coefficient write for ch1 | |
| | | b'1 | Enable coefficient write for ch1 | |
| CH2 | Coefficient write enable | b'0 | Disable coefficient write for ch2 | |
| | | b'1 | Enable coefficient write for ch2 | |
| CH3 | Coefficient write enable | b'0 | Disable coefficient write for ch3 | |
| | | b'1 | Enable coefficient write for ch3 | |
| PEQ | Coefficient write enable | b'0 | Disable coefficient write for PEQ | |
| | | b'1 | Enable coefficient write for PEQ | |

Ref) In convenience, a device programmer can write same biquad filter coefficients for CH1 and CH2 at a single time by setting Reg 0x7E as "x03".

B. Configuration Register Value Reference

Master & Channel Volume

| Index | dB | Index | dB | Index | dB | Index | dB | Index | dB | Index | dB |
|-------|------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| FF | 24 | D4 | 2.5 | A9 | -19 | 7E | -40.5 | 53 | -62 | 28 | -83.5 |
| FE | 23.5 | D3 | 2 | A8 | -19.5 | 7D | -41 | 52 | -62.5 | 27 | -84 |
| FD | 23 | D2 | 1.5 | A7 | -20 | 7C | -41.5 | 51 | -63 | 26 | -84.5 |
| FC | 22.5 | D1 | 1 | A6 | -20.5 | 7B | -42 | 50 | -63.5 | 25 | -85 |
| FB | 22 | D0 | 0.5 | A5 | -21 | 7A | -42.5 | 4F | -64 | 24 | -85.5 |
| FA | 21.5 | CF | 0 | A4 | -21.5 | 79 | -43 | 4E | -64.5 | 23 | -86 |
| F9 | 21 | CE | -0.5 | A3 | -22 | 78 | -43.5 | 4D | -65 | 22 | -86.5 |
| F8 | 20.5 | CD | -1 | A2 | -22.5 | 77 | -44 | 4C | -65.5 | 21 | -87 |
| F7 | 20 | CC | -1.5 | A1 | -23 | 76 | -44.5 | 4B | -66 | 20 | -87.5 |
| F6 | 19.5 | CB | -2 | A0 | -23.5 | 75 | -45 | 4A | -66.5 | 1F | -88 |
| F5 | 19 | CA | -2.5 | 9F | -24 | 74 | -45.5 | 49 | -67 | 1E | -88.5 |
| F4 | 18.5 | C9 | -3 | 9E | -24.5 | 73 | -46 | 48 | -67.5 | 1D | -89 |
| F3 | 18 | C8 | -3.5 | 9D | -25 | 72 | -46.5 | 47 | -68 | 1C | -89.5 |
| F2 | 17.5 | C7 | -4 | 9C | -25.5 | 71 | -47 | 46 | -68.5 | 1B | -90 |
| F1 | 17 | C6 | -4.5 | 9B | -26 | 70 | -47.5 | 45 | -69 | 1A | -90.5 |
| F0 | 16.5 | C5 | -5 | 9A | -26.5 | 6F | -48 | 44 | -69.5 | 19 | -91 |
| EF | 16 | C4 | -5.5 | 99 | -27 | 6E | -48.5 | 43 | -70 | 18 | -91.5 |
| EE | 15.5 | C3 | -6 | 98 | -27.5 | 6D | -49 | 42 | -70.5 | 17 | -92 |
| ED | 15 | C2 | -6.5 | 97 | -28 | 6C | -49.5 | 41 | -71 | 16 | -92.5 |
| EC | 14.5 | C1 | -7 | 96 | -28.5 | 6B | -50 | 40 | -71.5 | 15 | -93 |
| EB | 14 | C0 | -7.5 | 95 | -29 | 6A | -50.5 | 3F | -72 | 14 | -93.5 |
| EA | 13.5 | BF | -8 | 94 | -29.5 | 69 | -51 | 3E | -72.5 | 13 | -94 |
| E9 | 13 | BE | -8.5 | 93 | -30 | 68 | -51.5 | 3D | -73 | 12 | -94.5 |
| E8 | 12.5 | BD | -9 | 92 | -30.5 | 67 | -52 | 3C | -73.5 | 11 | -95 |
| E7 | 12 | BC | -9.5 | 91 | -31 | 66 | -52.5 | 3B | -74 | 10 | -95.5 |
| E6 | 11.5 | BB | -10 | 90 | -31.5 | 65 | -53 | 3A | -74.5 | 0F | -96 |
| E5 | 11 | BA | -10.5 | 8F | -32 | 64 | -53.5 | 39 | -75 | 0E | -96.5 |
| E4 | 10.5 | B9 | -11 | 8E | -32.5 | 63 | -54 | 38 | -75.5 | 0D | -97 |
| E3 | 10 | B8 | -11.5 | 8D | -33 | 62 | -54.5 | 37 | -76 | 0C | -97.5 |
| E2 | 9.5 | B7 | -12 | 8C | -33.5 | 61 | -55 | 36 | -76.5 | 0B | -98 |
| E1 | 9 | B6 | -12.5 | 8B | -34 | 60 | -55.5 | 35 | -77 | 0A | -98.5 |
| E0 | 8.5 | B5 | -13 | 8A | -34.5 | 5F | -56 | 34 | -77.5 | 9 | -99 |
| DF | 8 | B4 | -13.5 | 89 | -35 | 5E | -56.5 | 33 | -78 | 8 | -99.5 |
| DE | 7.5 | B3 | -14 | 88 | -35.5 | 5D | -57 | 32 | -78.5 | 7 | -100 |
| DD | 7 | B2 | -14.5 | 87 | -36 | 5C | -57.5 | 31 | -79 | 6 | -110 |
| DC | 6.5 | B1 | -15 | 86 | -36.5 | 5B | -58 | 30 | -79.5 | 5 | -120 |
| DB | 6 | B0 | -15.5 | 85 | -37 | 5A | -58.5 | 2F | -80 | 4 | -130 |
| DA | 5.5 | AF | -16 | 84 | -37.5 | 59 | -59 | 2E | -80.5 | 3 | -140 |
| D9 | 5 | AE | -16.5 | 83 | -38 | 58 | -59.5 | 2D | -81 | 2 | -150 |
| D8 | 4.5 | AD | -17 | 82 | -38.5 | 57 | -60 | 2C | -81.5 | 1 | -150 |
| D7 | 4 | AC | -17.5 | 81 | -39 | 56 | -60.5 | 2B | -82 | 0 | -150 |
| D6 | 3.5 | AB | -18 | 80 | -39.5 | 55 | -61 | 2A | -82.5 | | |
| D5 | 3 | AA | -18.5 | 7F | -40 | 54 | -61.5 | 29 | -83 | | |

Mixer Gain & Polarity

| Index | Polarity | dB | Index | Polarity | dB | Index | Polarity | dB | Index | Polarity | dB |
|-------|----------|------|-------|----------|------|-------|----------|------|-------|----------|------|
| 7E | + | 18 | 7D | - | 18 | 3E | + | -4 | 3D | - | -4 |
| 7C | + | 17 | 7B | - | 17 | 3C | + | -4.5 | 3B | - | -4.5 |
| 7A | + | 16 | 79 | - | 16 | 3A | + | -5 | 39 | - | -5 |
| 78 | + | 15 | 77 | - | 15 | 38 | + | -5.5 | 37 | - | -5.5 |
| 76 | + | 14 | 75 | - | 14 | 36 | + | -6 | 35 | - | -6 |
| 74 | + | 13 | 73 | - | 13 | 34 | + | -7 | 33 | - | -7 |
| 72 | + | 12 | 71 | - | 12 | 32 | + | -8 | 31 | - | -8 |
| 70 | + | 11 | 6F | - | 11 | 30 | + | -9 | 2F | - | -9 |
| 6E | + | 10 | 6D | - | 10 | 2E | + | -10 | 2D | - | -10 |
| 6C | + | 9 | 6B | - | 9 | 2C | + | -11 | 2B | - | -11 |
| 6A | + | 8 | 69 | - | 8 | 2A | + | -12 | 29 | - | -12 |
| 68 | + | 7 | 67 | - | 7 | 28 | + | -13 | 27 | - | -13 |
| 66 | + | 6 | 65 | - | 6 | 26 | + | -14 | 25 | - | -14 |
| 64 | + | 5.5 | 63 | - | 5.5 | 24 | + | -15 | 23 | - | -15 |
| 62 | + | 5 | 61 | - | 5 | 22 | + | -16 | 21 | - | -16 |
| 60 | + | 4.5 | 5F | - | 4.5 | 20 | + | -17 | 1F | - | -17 |
| 5E | + | 4 | 5D | - | 4 | 1E | + | -18 | 1D | - | -18 |
| 5C | + | 3.5 | 5B | - | 3.5 | 1C | + | -19 | 1B | - | -19 |
| 5A | + | 3 | 59 | - | 3 | 1A | + | -20 | 19 | - | -20 |
| 58 | + | 2.5 | 57 | - | 2.5 | 18 | + | -21 | 17 | - | -21 |
| 56 | + | 2 | 55 | - | 2 | 16 | + | -22 | 15 | - | -22 |
| 54 | + | 1.5 | 53 | - | 1.5 | 14 | + | -23 | 13 | - | -23 |
| 52 | + | 1 | 51 | - | 1 | 12 | + | -24 | 11 | - | -24 |
| 50 | + | 0.5 | 4F | - | 0.5 | 10 | + | -25 | 0F | - | -25 |
| 4E | + | 0 | 4D | - | 0 | 0E | + | -26 | 0D | - | -26 |
| 4C | + | -0.5 | 4B | - | -0.5 | 0C | + | -27 | 0B | - | -27 |
| 4A | + | -1 | 49 | - | -1 | 0A | + | -28 | 09 | - | -28 |
| 48 | + | -1.5 | 47 | - | -1.5 | 08 | + | -29 | 07 | - | -29 |
| 46 | + | -2 | 45 | - | -2 | 06 | + | -30 | 05 | - | -30 |
| 44 | + | -2.5 | 43 | - | -2.5 | 04 | + | -31 | 03 | - | -31 |
| 42 | + | -3 | 41 | - | -3 | 02 | + | -32 | 01 | - | -32 |
| 40 | + | -3.5 | 3F | - | -3.5 | 00 | + | -150 | | | |

Dynamic Range Control Threshold

| dB | Value | dB | Value | dB | Value | dB | Value |
|-----------|--------------|-----------|--------------|-----------|--------------|-----------|--------------|
| -57 | FF | -5.5 | DF | -2.3 | BF | 0.9 | 9F |
| -54 | FE | -5.4 | DE | -2.2 | BE | 1 | 9E |
| -51 | FD | -5.3 | DD | -2.1 | BD | 1.25 | 9D |
| -48 | FC | -5.2 | DC | -2 | BC | 1.5 | 9C |
| -45 | FB | -5.1 | DB | -1.9 | BB | 1.75 | 9B |
| -42 | FA | -5 | DA | -1.8 | BA | 2 | 9A |
| -39 | F9 | -4.9 | D9 | -1.7 | B9 | 2.25 | 99 |
| -36 | F8 | -4.8 | D8 | -1.6 | B8 | 2.5 | 98 |
| -33 | F7 | -4.7 | D7 | -1.5 | B7 | 2.75 | 97 |
| -30 | F6 | -4.6 | D6 | -1.4 | B6 | 3 | 96 |
| -27 | F5 | -4.5 | D5 | -1.3 | B5 | 3.25 | 95 |
| -24 | F4 | -4.4 | D4 | -1.2 | B4 | 3.5 | 94 |
| -21 | F3 | -4.3 | D3 | -1.1 | B3 | 3.75 | 93 |
| -18 | F2 | -4.2 | D2 | -1 | B2 | 4 | 92 |
| -15 | F1 | -4.1 | D1 | -0.9 | B1 | 4.25 | 91 |
| -12 | F0 | -4 | D0 | -0.8 | B0 | 4.5 | 90 |
| -11.5 | EF | -3.9 | CF | -0.7 | AF | 4.75 | 8F |
| -11 | EE | -3.8 | CE | -0.6 | AE | 5 | 8E |
| -10.5 | ED | -3.7 | CD | -0.5 | AD | 5.5 | 8D |
| -10 | EC | -3.6 | CC | -0.4 | AC | 6 | 8C |
| -9.5 | EB | -3.5 | CB | -0.3 | AB | 6.5 | 8B |
| -9 | EA | -3.4 | CA | -0.2 | AA | 7 | 8A |
| -8.5 | E9 | -3.3 | C9 | -0.1 | A9 | 7.5 | 89 |
| -8 | E8 | -3.2 | C8 | 0 | A8 | 8 | 88 |
| -7.5 | E7 | -3.1 | C7 | 0.1 | A7 | 8.5 | 87 |
| -7 | E6 | -3 | C6 | 0.2 | A6 | 9 | 86 |
| -6.5 | E5 | -2.9 | C5 | 0.3 | A5 | 9.5 | 85 |
| -6 | E4 | -2.8 | C4 | 0.4 | A4 | 10 | 84 |
| -5.9 | E3 | -2.7 | C3 | 0.5 | A3 | 10.5 | 83 |
| -5.8 | E2 | -2.6 | C2 | 0.6 | A2 | 11 | 82 |
| -5.7 | E1 | -2.5 | C1 | 0.7 | A1 | 11.5 | 81 |
| -5.6 | E0 | -2.4 | C0 | 0.8 | A0 | 12 | 80 |

※ CPR bit = 1

Auto Mute Detection Threshold Table

| Name | Description | Value | dB |
|-------------|-------------------------------------|--------------|------------------|
| AT | Auto-mute Detection threshold | 0000 | -126 |
| | | 0001 | -120 |
| | | 0010 | -114 |
| | | 0011 | -108 |
| | | 0100 | -102 |
| | | 0101 | -96 |
| | | 0110 | -90 |
| | | 0111 | -84 |
| | | 1000 | -78 |
| | | 1001 | -72 |
| | | 1010 | -66 |
| | | 1011 | -60 |
| | | 1100 | -54 |
| | | 1101 | -48 |
| | | 1110 | -42 |
| | | 1111 | Auto-mute |

※ Do not use value 1111.

Power Meter Reading Table

| addr 0x54 | addr 0x54 | Db | addr 0x54 | addr 0x54 | Db | addr 0x54 | addr 0x54 | dB | addr 0x54 | addr 0x54 | dB |
|-----------|-----------|-------|-----------|-----------|-------|-----------|-----------|-------|-----------|-----------|--------|
| 0 | 0x00 | -0.0 | 64 | 0x40 | -32.0 | 128 | 0x80 | -64.0 | 192 | 0xC0 | -96.0 |
| 1 | 0x01 | -0.5 | 65 | 0x41 | -32.5 | 129 | 0x81 | -64.5 | 193 | 0xC1 | -96.5 |
| 2 | 0x02 | -1.0 | 66 | 0x42 | -33.0 | 130 | 0x82 | -65.0 | 194 | 0xC2 | -97.0 |
| 3 | 0x03 | -1.5 | 67 | 0x43 | -33.5 | 131 | 0x83 | -65.5 | 195 | 0xC3 | -97.5 |
| 4 | 0x04 | -2.0 | 68 | 0x44 | -34.0 | 132 | 0x84 | -66.0 | 196 | 0xC4 | -98.0 |
| 5 | 0x05 | -2.5 | 69 | 0x45 | -34.5 | 133 | 0x85 | -66.5 | 197 | 0xC5 | -98.5 |
| 6 | 0x06 | -3.0 | 70 | 0x46 | -35.0 | 134 | 0x86 | -67.0 | 198 | 0xC6 | -99.0 |
| 7 | 0x07 | -3.5 | 71 | 0x47 | -35.5 | 135 | 0x87 | -67.5 | 199 | 0xC7 | -99.5 |
| 8 | 0x08 | -4.0 | 72 | 0x48 | -36.0 | 136 | 0x88 | -68.0 | 200 | 0xC8 | -100.0 |
| 9 | 0x09 | -4.5 | 73 | 0x49 | -36.5 | 137 | 0x89 | -68.5 | 201 | 0xC9 | -100.5 |
| 10 | 0x0A | -5.0 | 74 | 0x4A | -37.0 | 138 | 0x8A | -69.0 | 202 | 0xCA | -101.0 |
| 11 | 0x0B | -5.5 | 75 | 0x4B | -37.5 | 139 | 0x8B | -69.5 | 203 | 0xCB | -101.5 |
| 12 | 0x0C | -6.0 | 76 | 0x4C | -38.0 | 140 | 0x8C | -70.0 | 204 | 0xCC | -102.0 |
| 13 | 0x0D | -6.5 | 77 | 0x4D | -38.5 | 141 | 0x8D | -70.5 | 205 | 0xCD | -102.5 |
| 14 | 0x0E | -7.0 | 78 | 0x4E | -39.0 | 142 | 0x8E | -71.0 | 206 | 0xCE | -103.0 |
| 15 | 0x0F | -7.5 | 79 | 0x4F | -39.5 | 143 | 0x8F | -71.5 | 207 | 0xCF | -103.5 |
| 16 | 0x10 | -8.0 | 80 | 0x50 | -40.0 | 144 | 0x90 | -72.0 | 208 | 0xD0 | -104.0 |
| 17 | 0x11 | -8.5 | 81 | 0x51 | -40.5 | 145 | 0x91 | -72.5 | 209 | 0xD1 | -104.5 |
| 18 | 0x12 | -9.0 | 82 | 0x52 | -41.0 | 146 | 0x92 | -73.0 | 210 | 0xD2 | -105.0 |
| 19 | 0x13 | -9.5 | 83 | 0x53 | -41.5 | 147 | 0x93 | -73.5 | 211 | 0xD3 | -105.5 |
| 20 | 0x14 | -10.0 | 84 | 0x54 | -42.0 | 148 | 0x94 | -74.0 | 212 | 0xD4 | -106.0 |
| 21 | 0x15 | -10.5 | 85 | 0x55 | -42.5 | 149 | 0x95 | -74.5 | 213 | 0xD5 | -106.5 |
| 22 | 0x16 | -11.0 | 86 | 0x56 | -43.0 | 150 | 0x96 | -75.0 | 214 | 0xD6 | -107.0 |
| 23 | 0x17 | -11.5 | 87 | 0x57 | -43.5 | 151 | 0x97 | -75.5 | 215 | 0xD7 | -107.5 |
| 24 | 0x18 | -12.0 | 88 | 0x58 | -44.0 | 152 | 0x98 | -76.0 | 216 | 0xD8 | -108.0 |
| 25 | 0x19 | -12.5 | 89 | 0x59 | -44.5 | 153 | 0x99 | -76.5 | 217 | 0xD9 | -108.5 |
| 26 | 0x1A | -13.0 | 90 | 0x5A | -45.0 | 154 | 0x9A | -77.0 | 218 | 0xDA | -109.0 |
| 27 | 0x1B | -13.5 | 91 | 0x5B | -45.5 | 155 | 0x9B | -77.5 | 219 | 0xDB | -109.5 |
| 28 | 0x1C | -14.0 | 92 | 0x5C | -46.0 | 156 | 0x9C | -78.0 | 220 | 0xDC | -110.0 |
| 29 | 0x1D | -14.5 | 93 | 0x5D | -46.5 | 157 | 0x9D | -78.5 | 221 | 0xDD | -110.5 |
| 30 | 0x1E | -15.0 | 94 | 0x5E | -47.0 | 158 | 0x9E | -79.0 | 222 | 0xDE | -111.0 |
| 31 | 0x1F | -15.5 | 95 | 0x5F | -47.5 | 159 | 0x9F | -79.5 | 223 | 0xDF | -111.5 |
| 32 | 0x20 | -16.0 | 96 | 0x60 | -48.0 | 160 | 0xA0 | -80.0 | 224 | 0xE0 | -112.0 |
| 33 | 0x21 | -16.5 | 97 | 0x61 | -48.5 | 161 | 0xA1 | -80.5 | 225 | 0xE1 | -112.5 |
| 34 | 0x22 | -17.0 | 98 | 0x62 | -49.0 | 162 | 0xA2 | -81.0 | 226 | 0xE2 | -113.0 |
| 35 | 0x23 | -17.5 | 99 | 0x63 | -49.5 | 163 | 0xA3 | -81.5 | 227 | 0xE3 | -113.5 |
| 36 | 0x24 | -18.0 | 100 | 0x64 | -50.0 | 164 | 0xA4 | -82.0 | 228 | 0xE4 | -114.0 |
| 37 | 0x25 | -18.5 | 101 | 0x65 | -50.5 | 165 | 0xA5 | -82.5 | 229 | 0xE5 | -114.5 |
| 38 | 0x26 | -19.0 | 102 | 0x66 | -51.0 | 166 | 0xA6 | -83.0 | 230 | 0xE6 | -115.0 |
| 39 | 0x27 | -19.5 | 103 | 0x67 | -51.5 | 167 | 0xA7 | -83.5 | 231 | 0xE7 | -115.5 |
| 40 | 0x28 | -20.0 | 104 | 0x68 | -52.0 | 168 | 0xA8 | -84.0 | 232 | 0xE8 | -116.0 |
| 41 | 0x29 | -20.5 | 105 | 0x69 | -52.5 | 169 | 0xA9 | -84.5 | 233 | 0xE9 | -116.5 |
| 42 | 0x2A | -21.0 | 106 | 0x6A | -53.0 | 170 | 0xAA | -85.0 | 234 | 0xEA | -117.0 |
| 43 | 0x2B | -21.5 | 107 | 0x6B | -53.5 | 171 | 0xAB | -85.5 | 235 | 0xEB | -117.5 |
| 44 | 0x2C | -22.0 | 108 | 0x6C | -54.0 | 172 | 0xAC | -86.0 | 236 | 0xEC | -118.0 |
| 45 | 0x2D | -22.5 | 109 | 0x6D | -54.5 | 173 | 0xAD | -86.5 | 237 | 0xED | -118.5 |
| 46 | 0x2E | -23.0 | 110 | 0x6E | -55.0 | 174 | 0xAE | -87.0 | 238 | 0xEE | -119.0 |
| 47 | 0x2F | -23.5 | 111 | 0x6F | -55.5 | 175 | 0xAF | -87.5 | 239 | 0xEF | -119.5 |
| 48 | 0x30 | -24.0 | 112 | 0x70 | -56.0 | 176 | 0xB0 | -88.0 | 240 | 0xF0 | -120.0 |
| 49 | 0x31 | -24.5 | 113 | 0x71 | -56.5 | 177 | 0xB1 | -88.5 | 241 | 0xF1 | -120.5 |
| 50 | 0x32 | -25.0 | 114 | 0x72 | -57.0 | 178 | 0xB2 | -89.0 | 242 | 0xF2 | -121.0 |
| 51 | 0x33 | -25.5 | 115 | 0x73 | -57.5 | 179 | 0xB3 | -89.5 | 243 | 0xF3 | -121.5 |
| 52 | 0x34 | -26.0 | 116 | 0x74 | -58.0 | 180 | 0xB4 | -90.0 | 244 | 0xF4 | -122.0 |
| 53 | 0x35 | -26.5 | 117 | 0x75 | -58.5 | 181 | 0xB5 | -90.5 | 245 | 0xF5 | -122.5 |
| 54 | 0x36 | -27.0 | 118 | 0x76 | -59.0 | 182 | 0xB6 | -91.0 | 246 | 0xF6 | -123.0 |
| 55 | 0x37 | -27.5 | 119 | 0x77 | -59.5 | 183 | 0xB7 | -91.5 | 247 | 0xF7 | -123.5 |
| 56 | 0x38 | -28.0 | 120 | 0x78 | -60.0 | 184 | 0xB8 | -92.0 | 248 | 0xF8 | -124.0 |
| 57 | 0x39 | -28.5 | 121 | 0x79 | -60.5 | 185 | 0xB9 | -92.5 | 249 | 0xF9 | -124.5 |
| 58 | 0x3A | -29.0 | 122 | 0x7A | -61.0 | 186 | 0xBA | -93.0 | 250 | 0xFA | -125.0 |
| 59 | 0x3B | -29.5 | 123 | 0x7B | -61.5 | 187 | 0xBB | -93.5 | 251 | 0xFB | -125.5 |
| 60 | 0x3C | -30.0 | 124 | 0x7C | -62.0 | 188 | 0xBC | -94.0 | 252 | 0xFC | -126.0 |
| 61 | 0x3D | -30.5 | 125 | 0x7D | -62.5 | 189 | 0xBD | -94.5 | 253 | 0xFD | -126.5 |
| 62 | 0x3E | -31.0 | 126 | 0x7E | -63.0 | 190 | 0xBE | -95.0 | 254 | 0xFE | -127.0 |
| 63 | 0x3F | -31.5 | 127 | 0x7F | -63.5 | 191 | 0xBF | -95.5 | 255 | 0xFF | -127.5 |

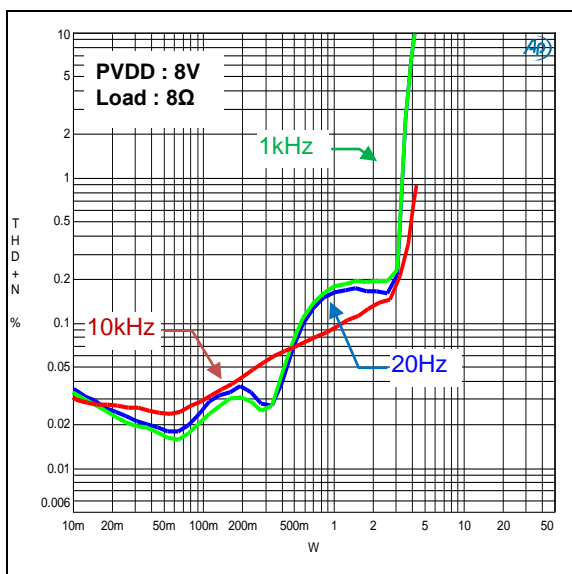
※ Output 8bit value : (-dB * 2) n dB = output 8bit *0.5

C. Typical Characteristics Graph

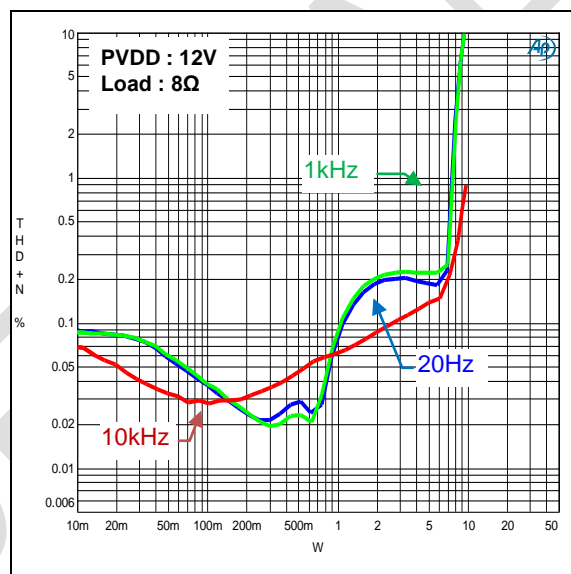
Total Harmonic Distortion + Noise vs. Power, BTL Configuration, 8Ω

※ Condition : 2Layer Board

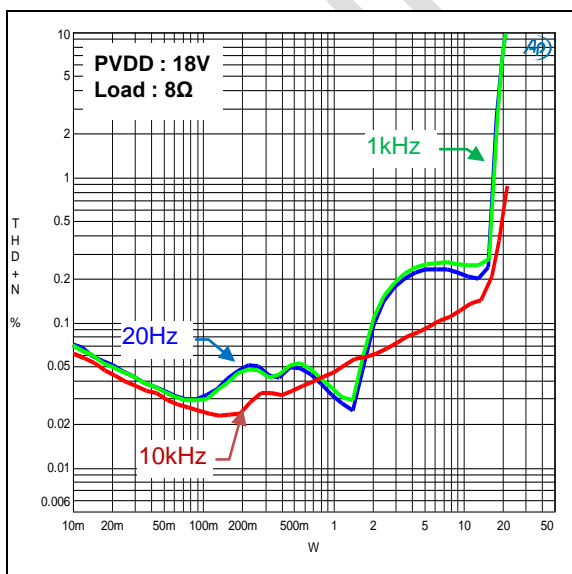
THD+N vs. Power



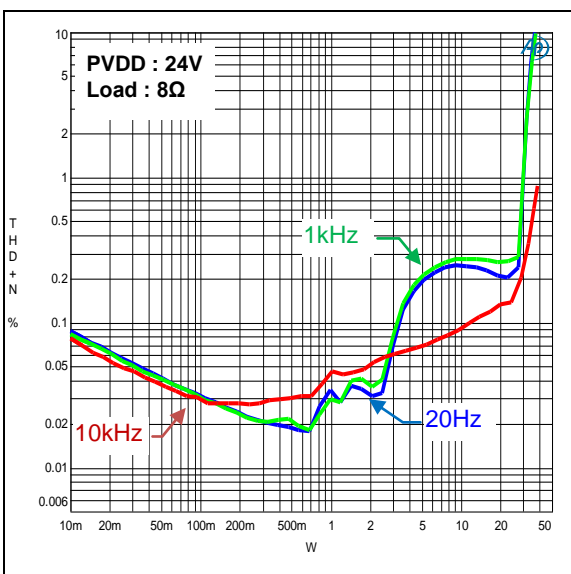
THD+N vs. Power



THD+N vs. Power

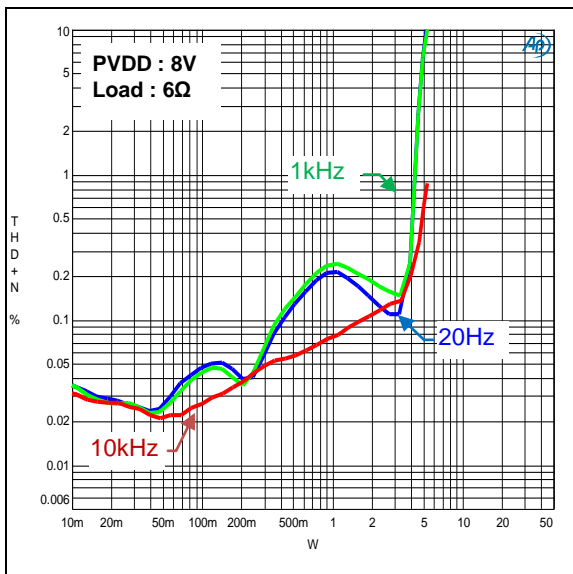


THD+N vs. Power

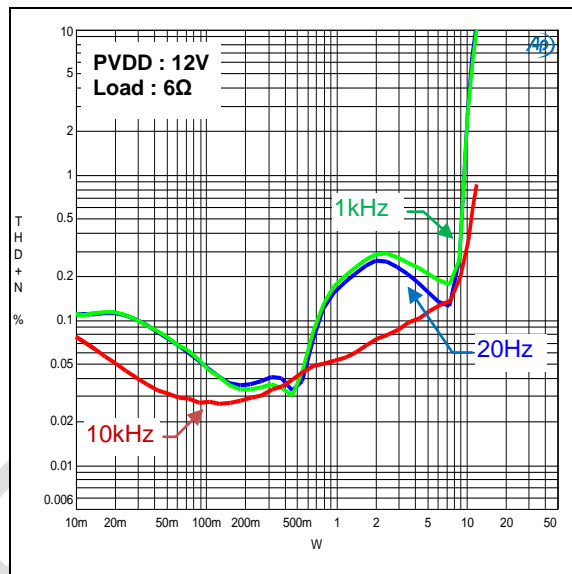


Total Harmonic Distortion + Noise vs. Power, BTL Configuration, 6Ω

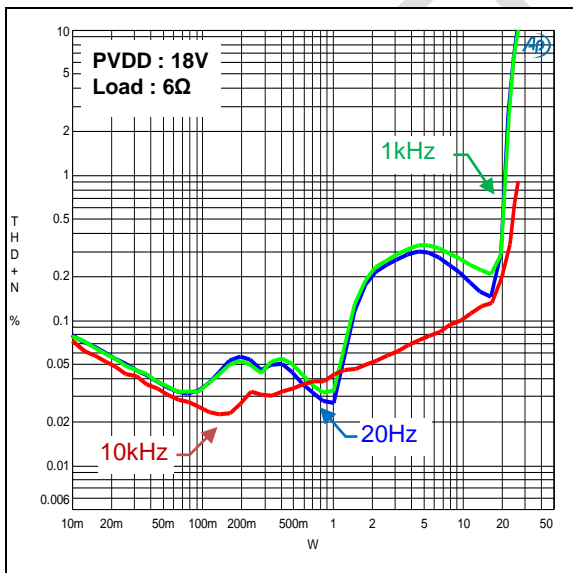
THD+N vs. Power



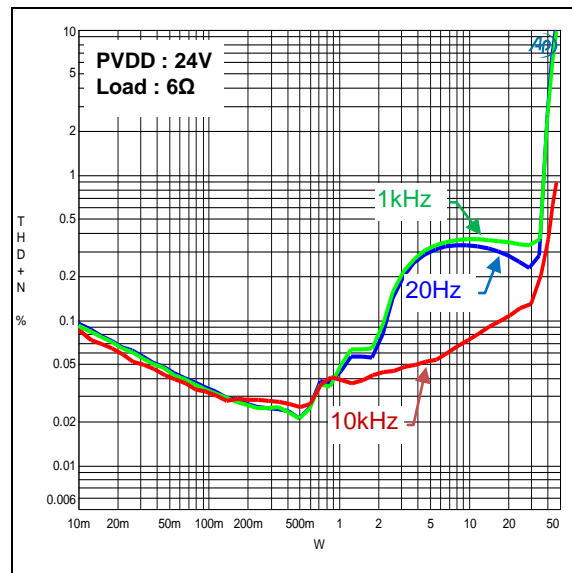
THD+N vs. Power



THD+N vs. Power

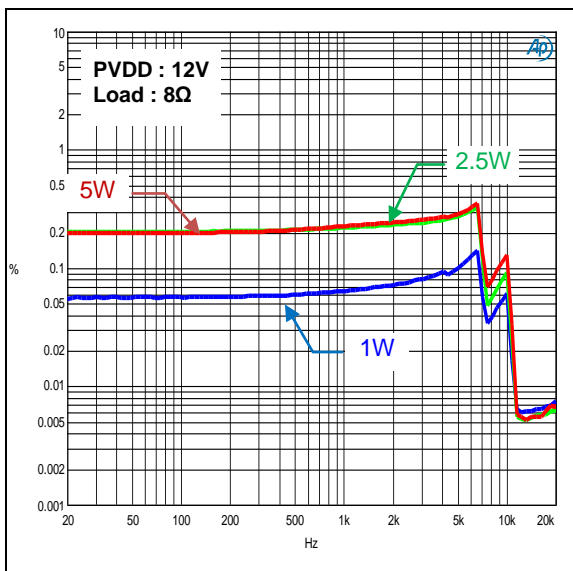


THD+N vs. Power

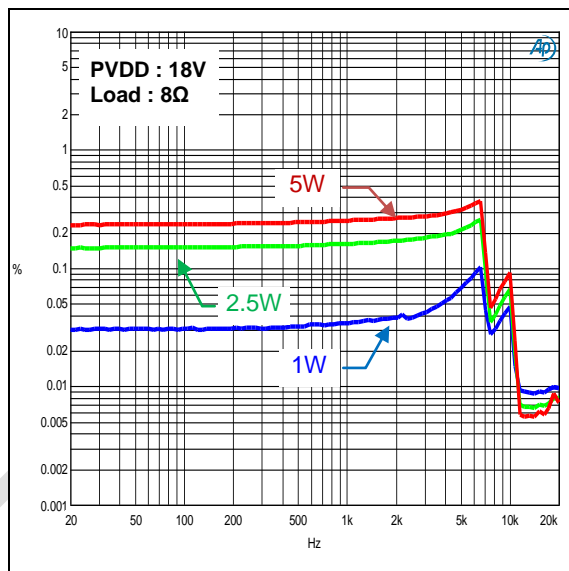


Total Harmonic Distortion + Noise vs. Frequency, BTL Configuration, 8Ω

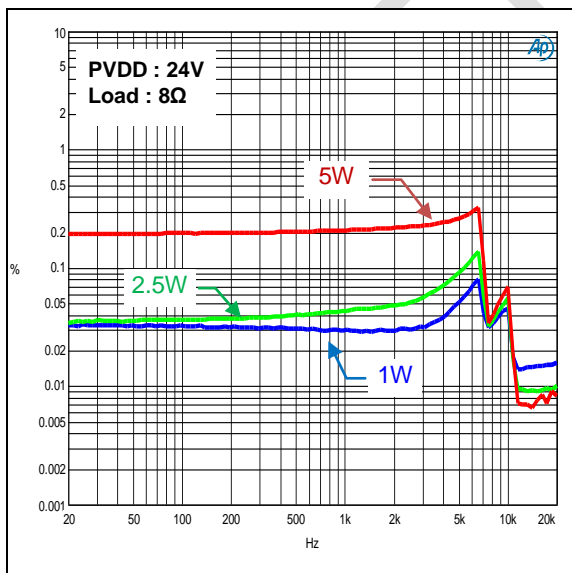
THD+N vs. Frequency



THD+N vs. Frequency

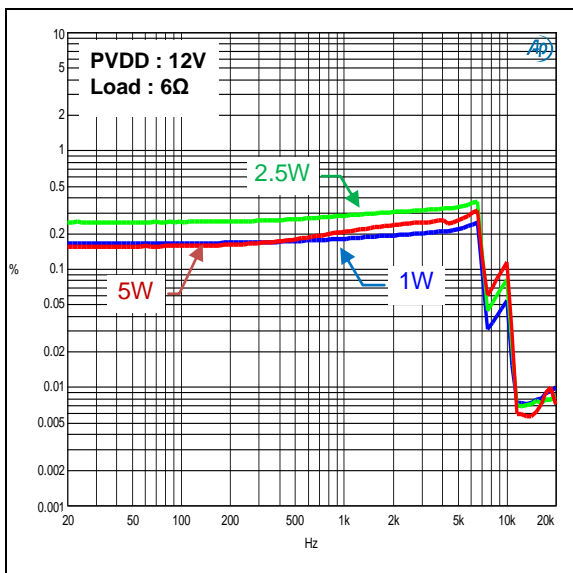


THD+N vs. Frequency

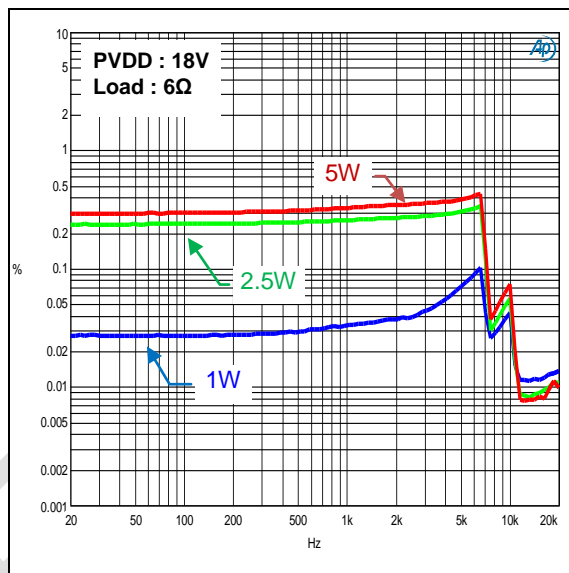


Total Harmonic Distortion + Noise vs. Frequency, BTL Configuration, 6Ω

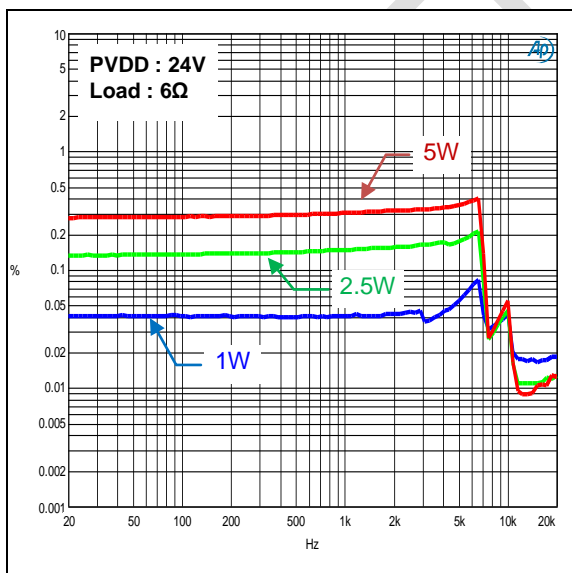
THD+N vs. Frequency



THD+N vs. Frequency



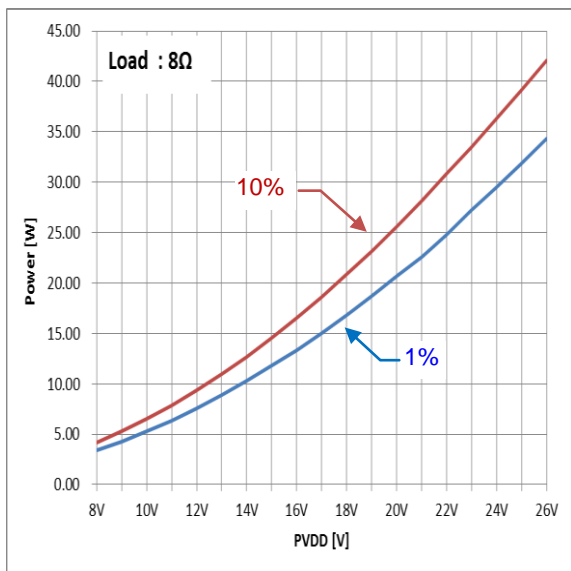
THD+N vs. Frequency



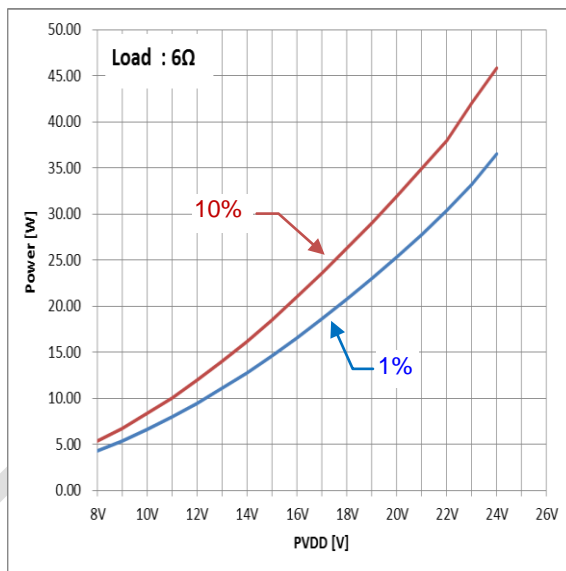
Output Power vs. PVDD, BTL Configuration

※ Condition : 2Layer Board

Output Power vs. PVDD

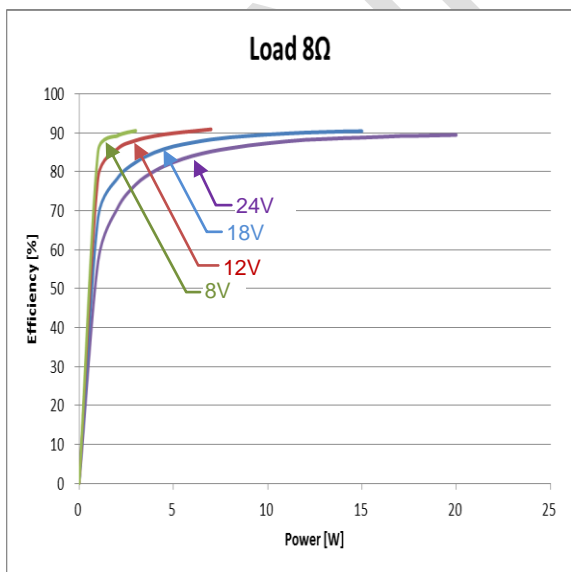


Output Power vs. PVDD

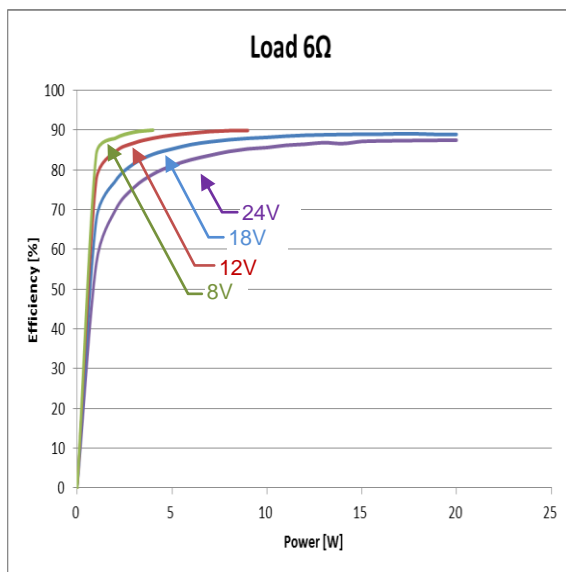


Efficiency vs. Total Power, BTL Configuration

Efficiency vs. Output Power

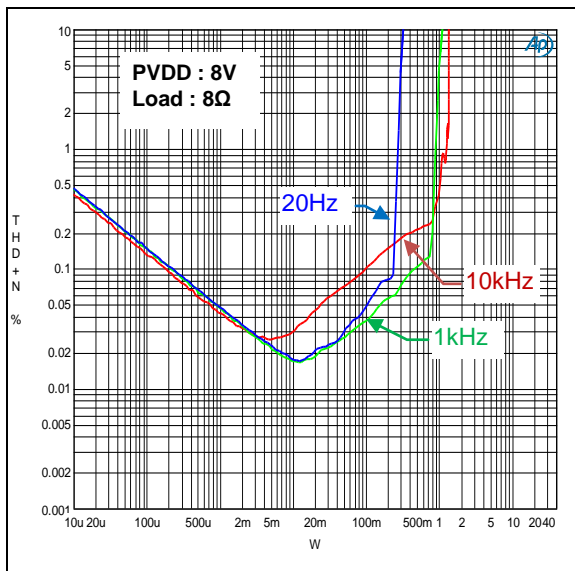


Efficiency vs. Output Power

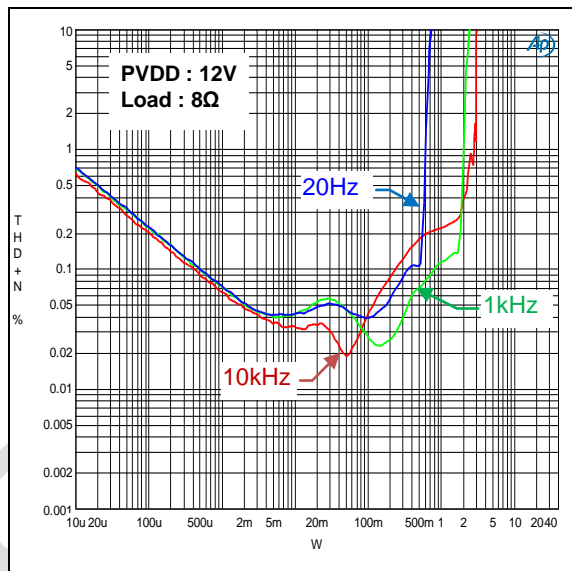


Total Harmonic Distortion + Noise vs. Power, SE Configuration, 8Ω

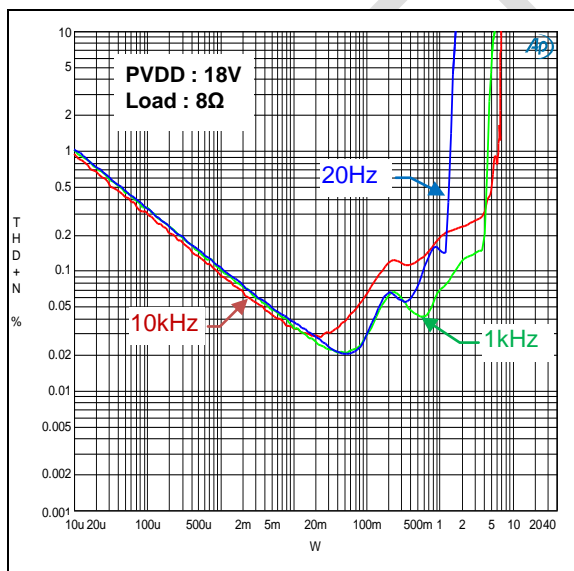
THD+N vs. Power



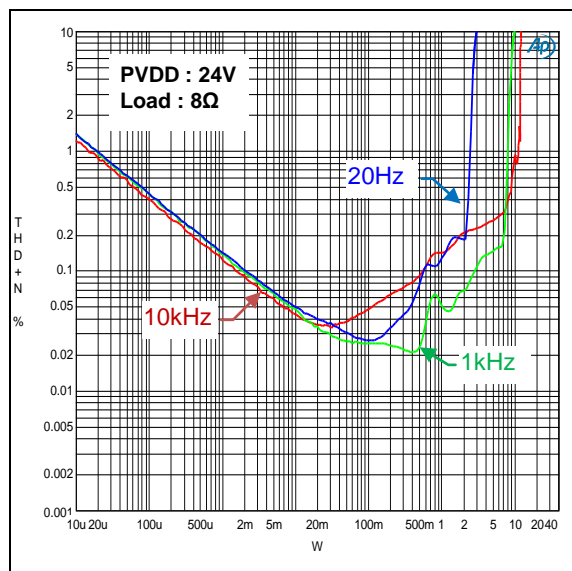
THD+N vs. Power



THD+N vs. Power

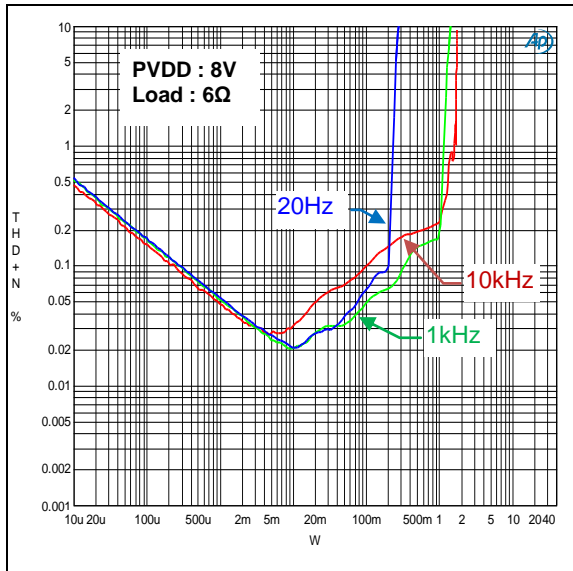


THD+N vs. Power

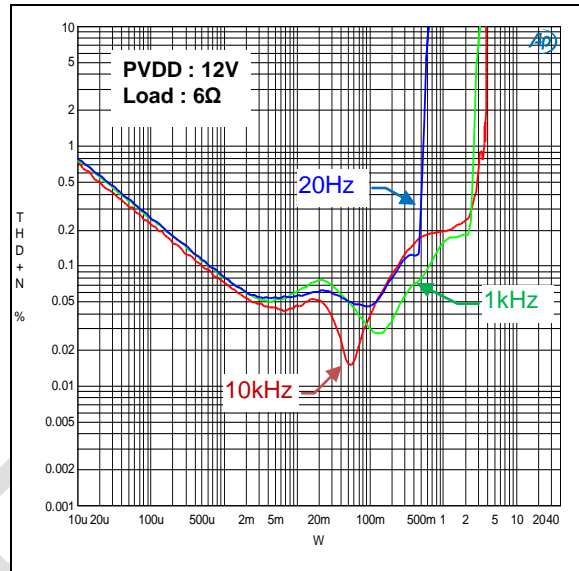


Total Harmonic Distortion + Noise vs. Power, SE Configuration, 6Ω

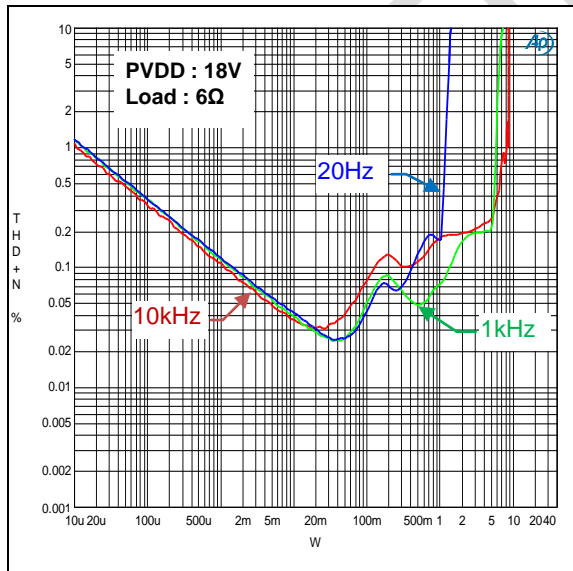
THD+N vs. Power



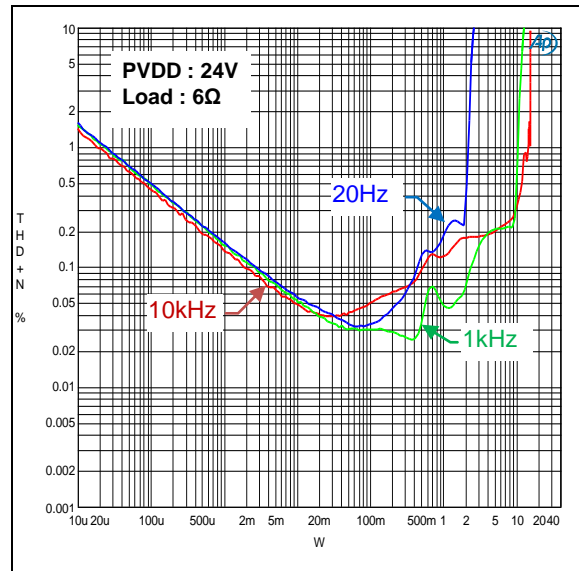
THD+N vs. Power



THD+N vs. Power

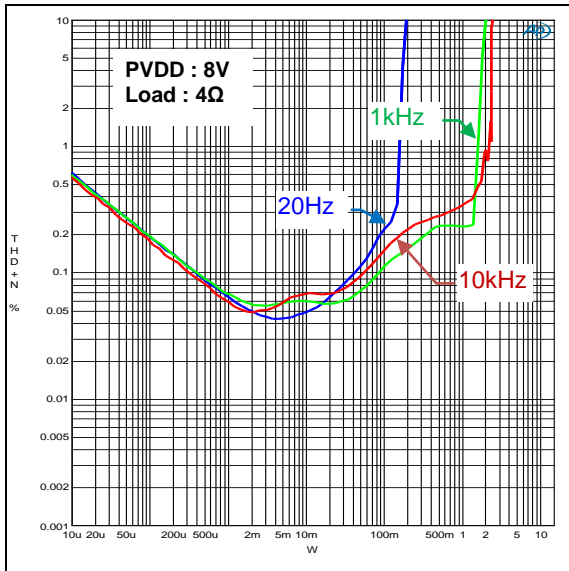


THD+N vs. Power

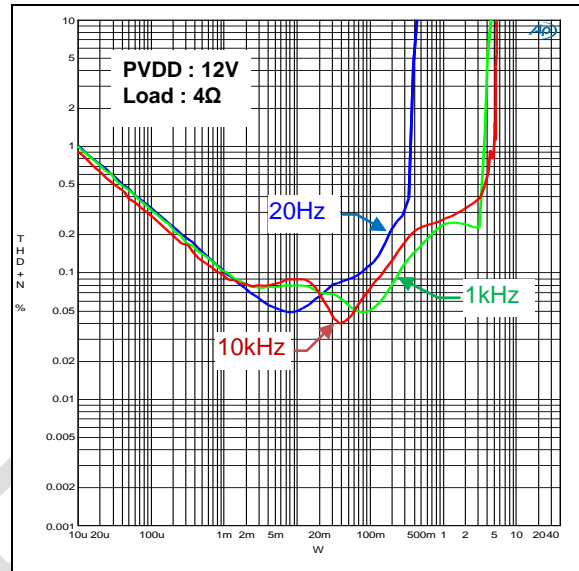


Total Harmonic Distortion + Noise vs. Power, SE Configuration, 4Ω

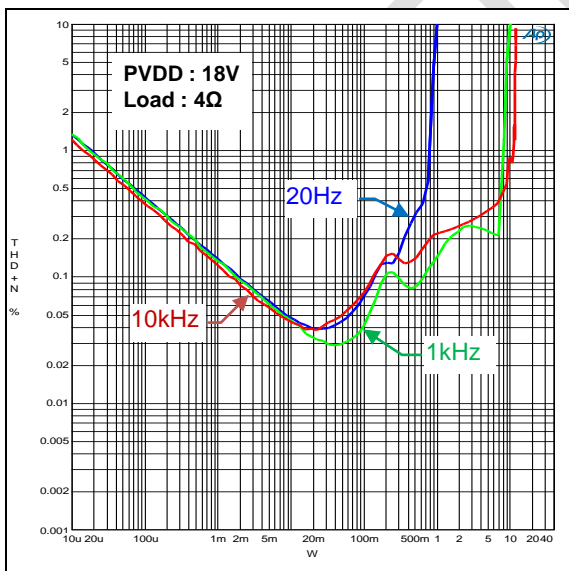
THD+N vs. Power



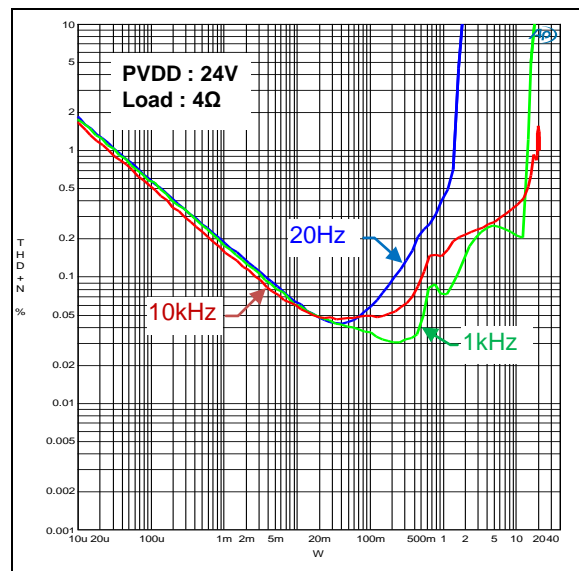
THD+N vs. Power



THD+N vs. Power

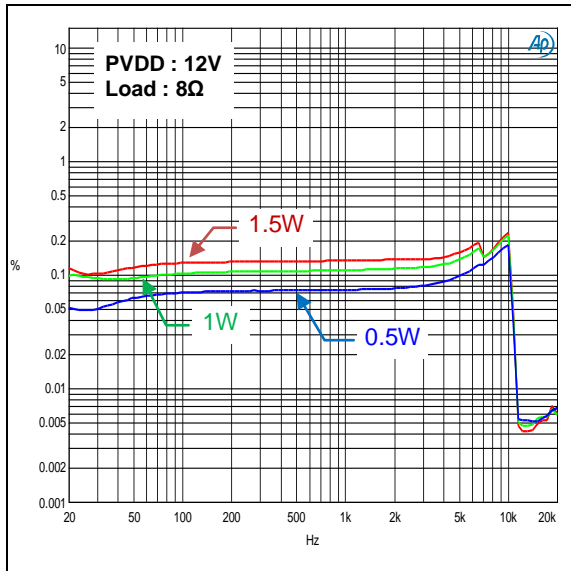


THD+N vs. Power

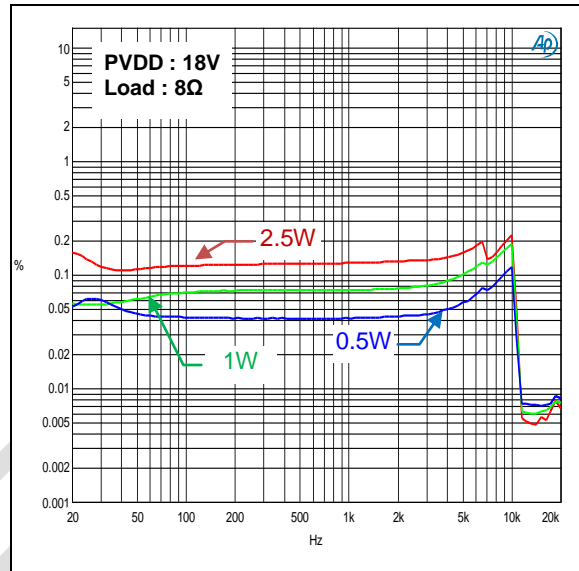


Total Harmonic Distortion + Noise vs. Frequency, SE Configuration, 8Ω

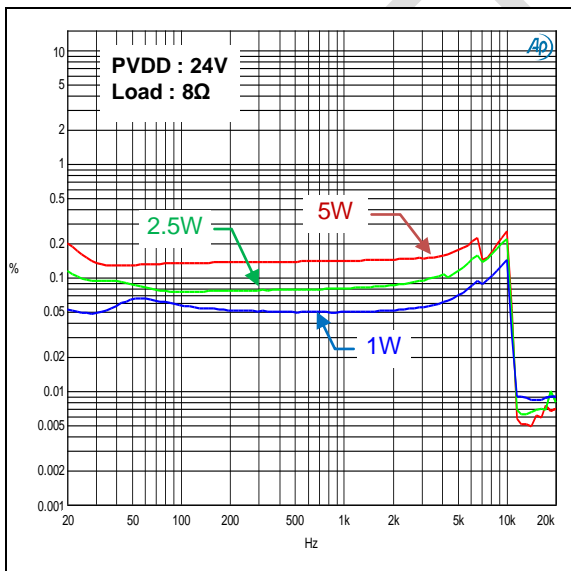
THD+N vs. Frequency



THD+N vs. Frequency

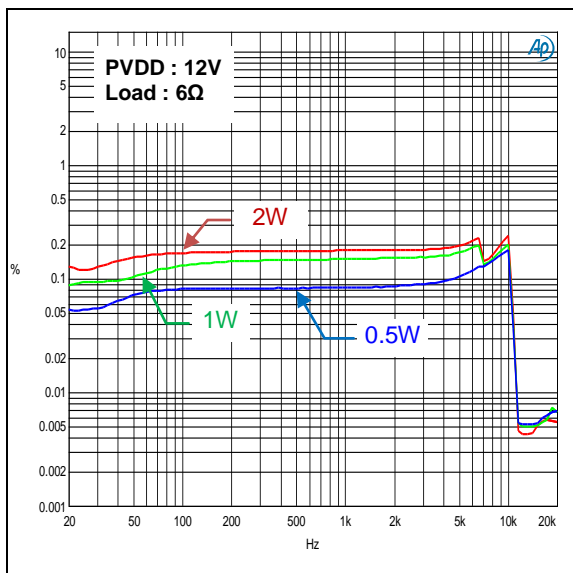


THD+N vs. Frequency

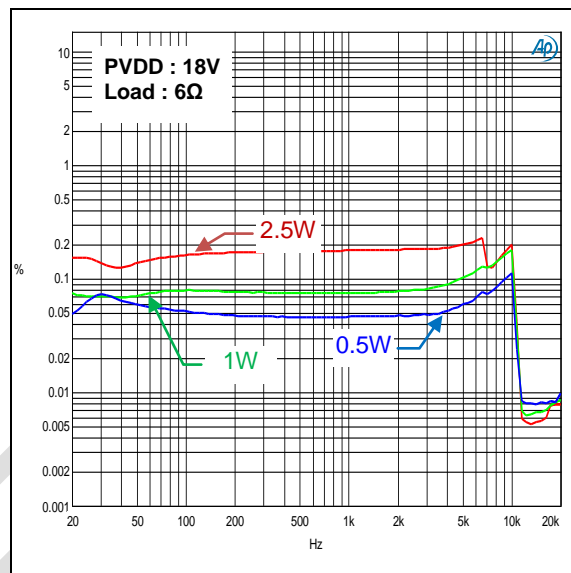


Total Harmonic Distortion + Noise vs. Frequency, SE Configuration, 6Ω

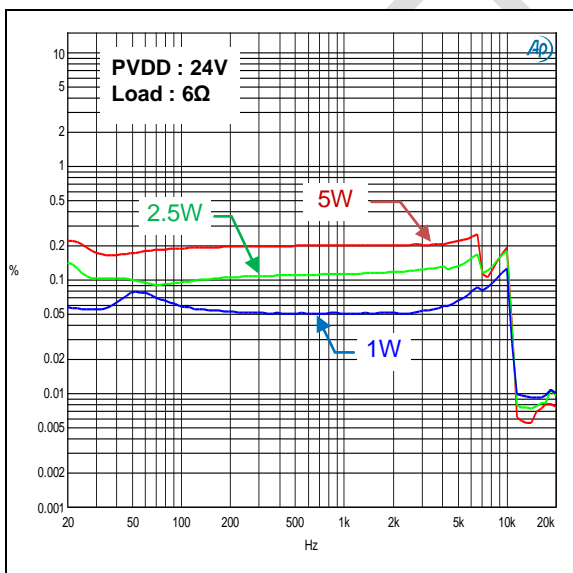
THD+N vs. Frequency



THD+N vs. Frequency

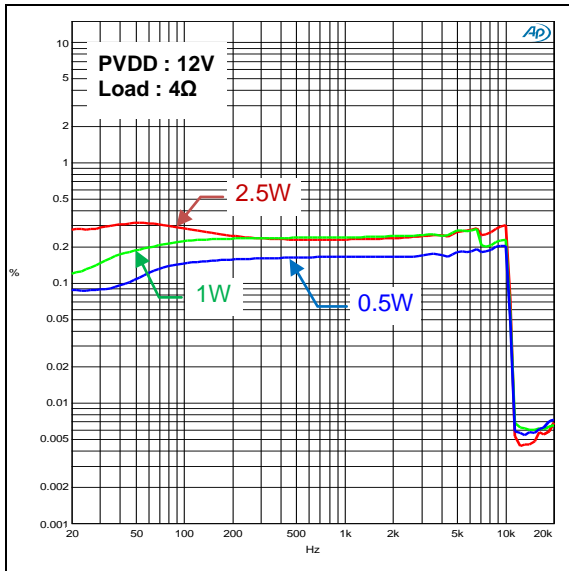


THD+N vs. Frequency

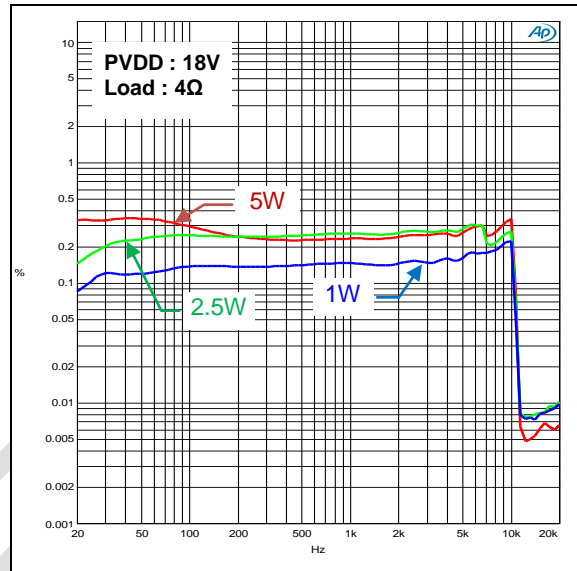


Total Harmonic Distortion + Noise vs. Frequency, SE Configuration, 4Ω

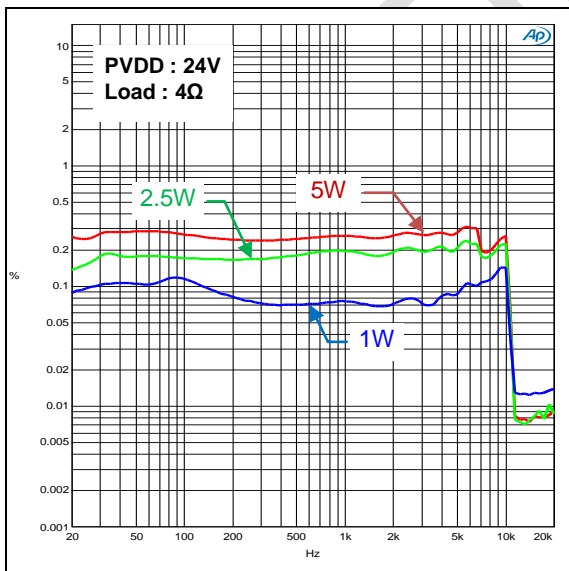
THD+N vs. Frequency



THD+N vs. Frequency

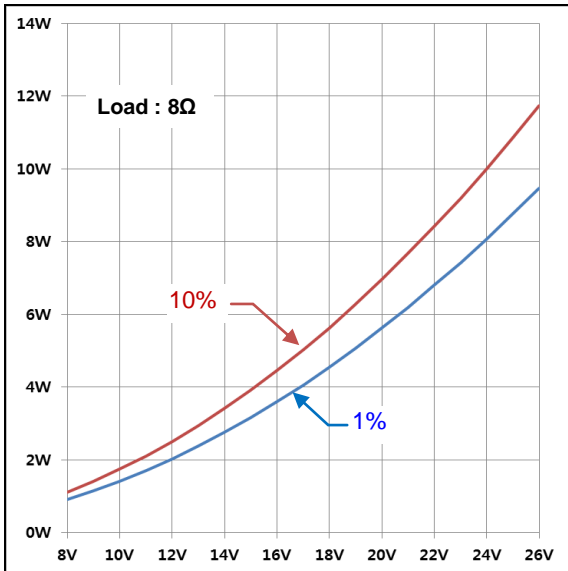


THD+N vs. Frequency

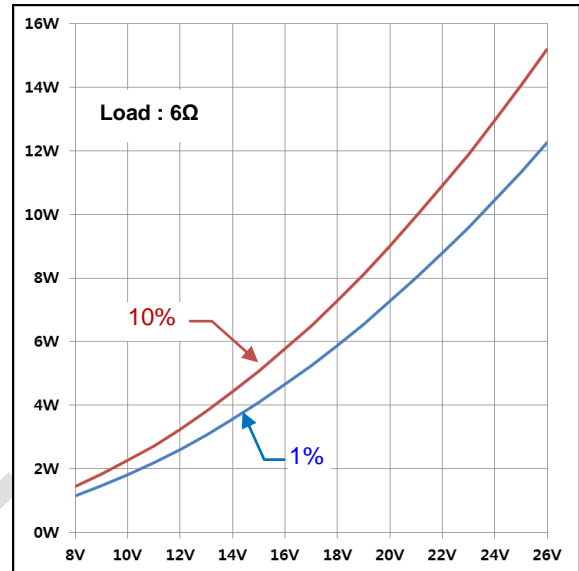


Output Power vs. PVDD, SE Configuration

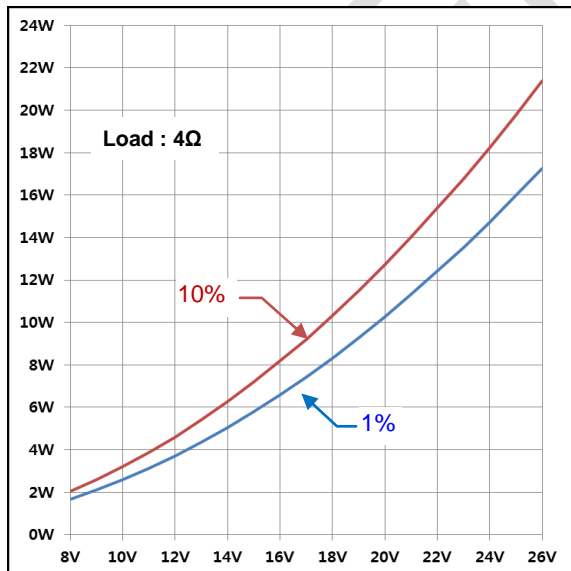
Output Power vs. PVDD



Output Power vs. PVDD

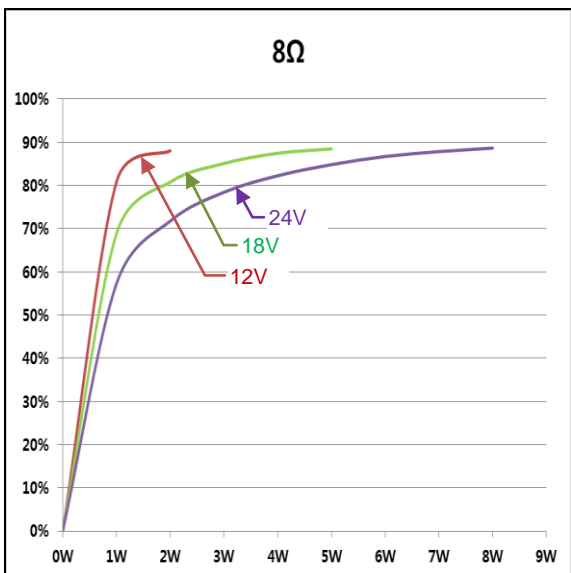


Output Power vs. PVDD

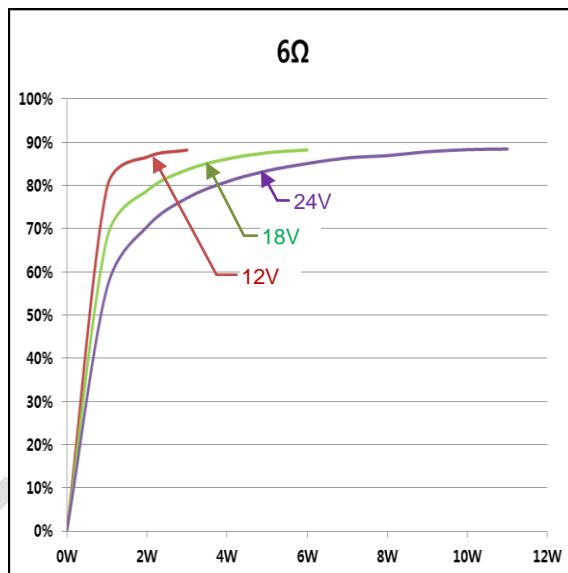


Efficiency vs. Total Power, SE Configuration

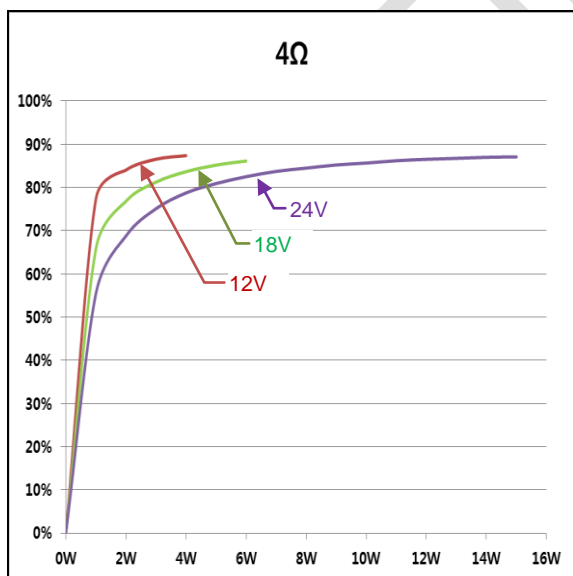
Efficiency vs. Output Power



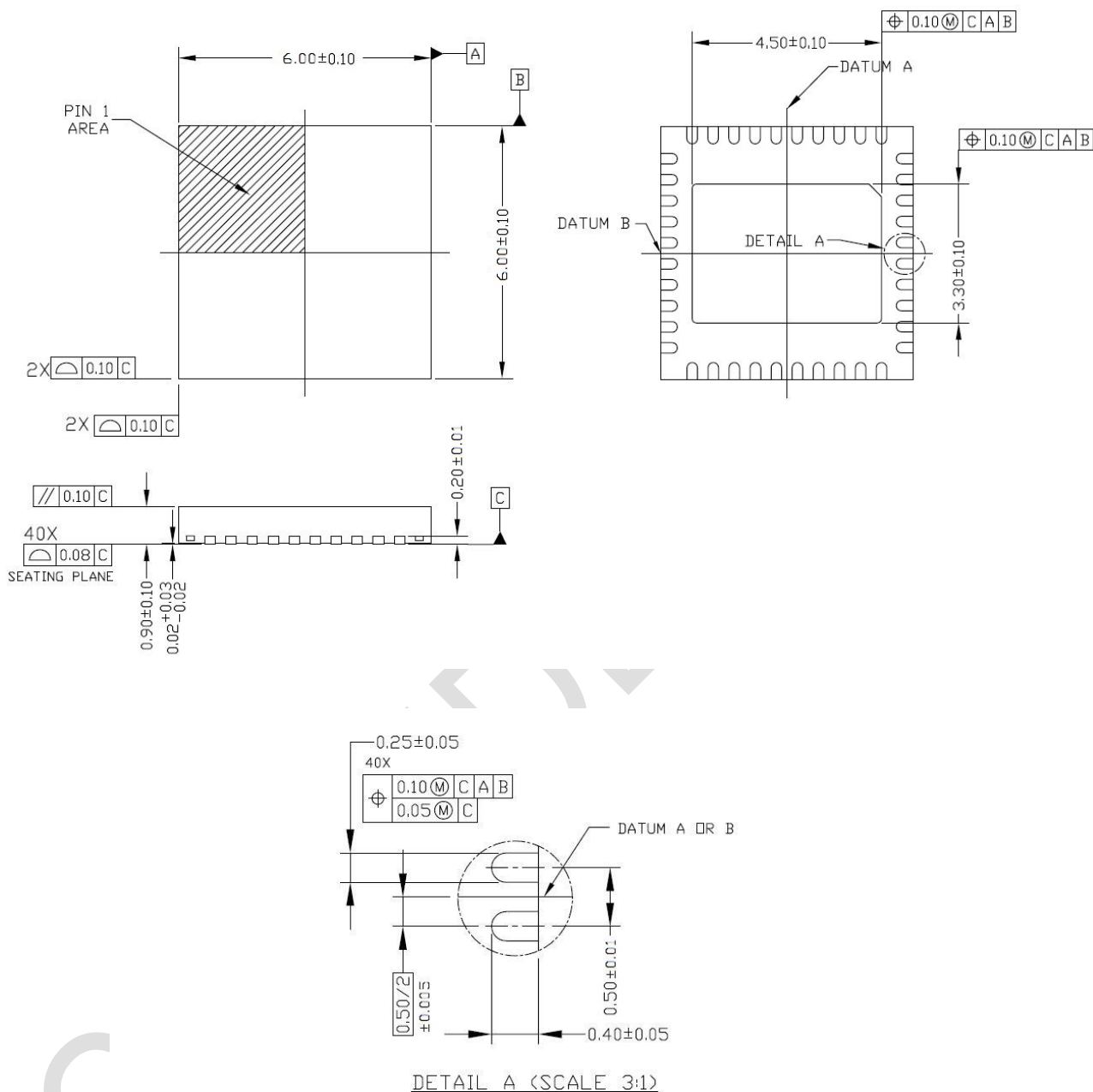
Efficiency vs. Output Power



Efficiency vs. Output Power



D. Outline and Mechanical Data



NOTES:

1. DIMENSIONING AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5-1994
ALL DIMENSIONS ARE IN MILLIMETERS * IN DEGREES
2. DIMENSION OF LEAD WIDTH APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP (BOTH ROWS). IF THE TERMINAL HAS OPTIONAL RADIUS ON THE END OF THE TERMINAL, THE LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA